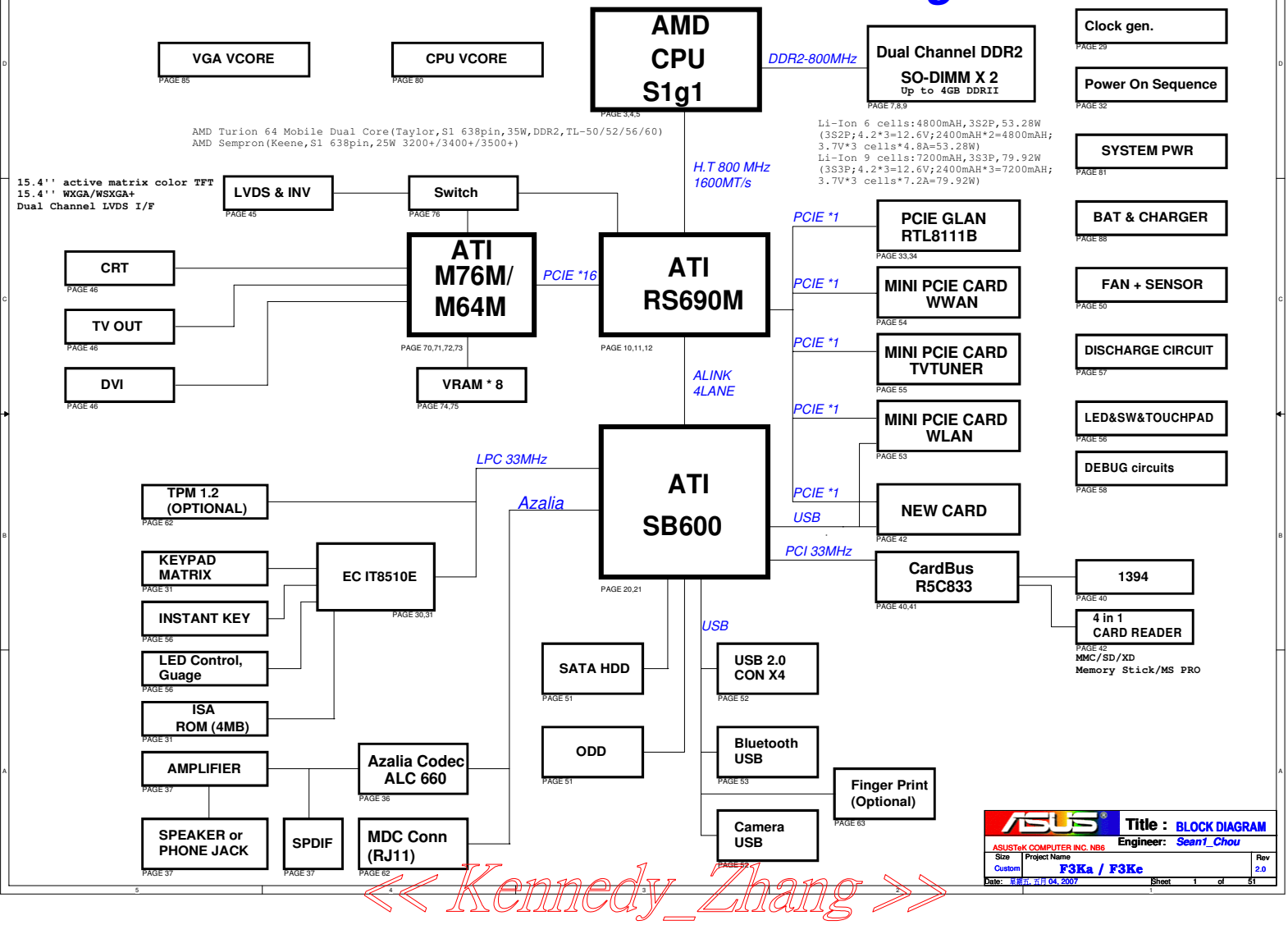
F3Ka/F3Ke Block Diagram



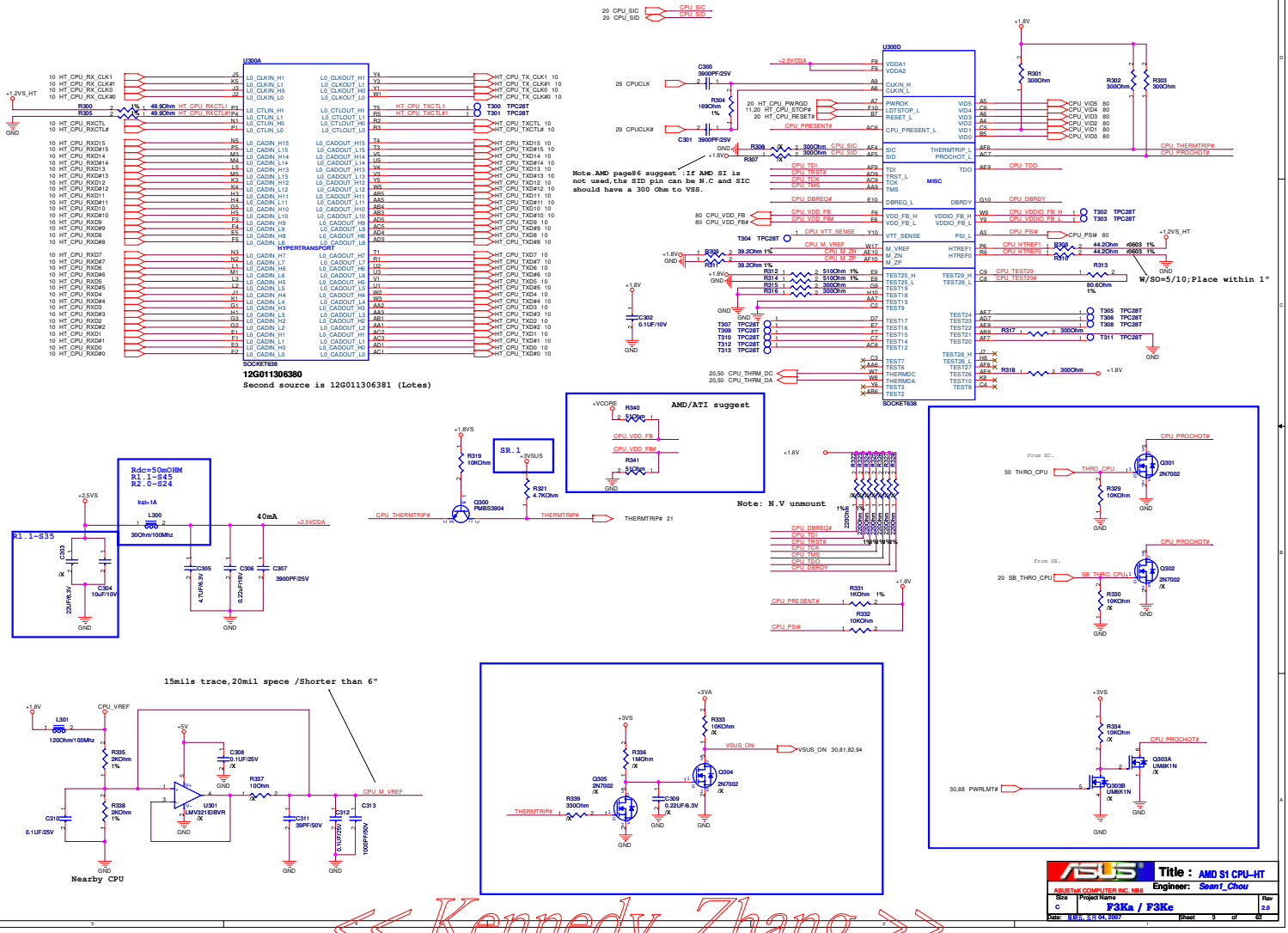
ASUSTeK COMPUTER INC. NB6

Title : BLOCK DIAGRAM

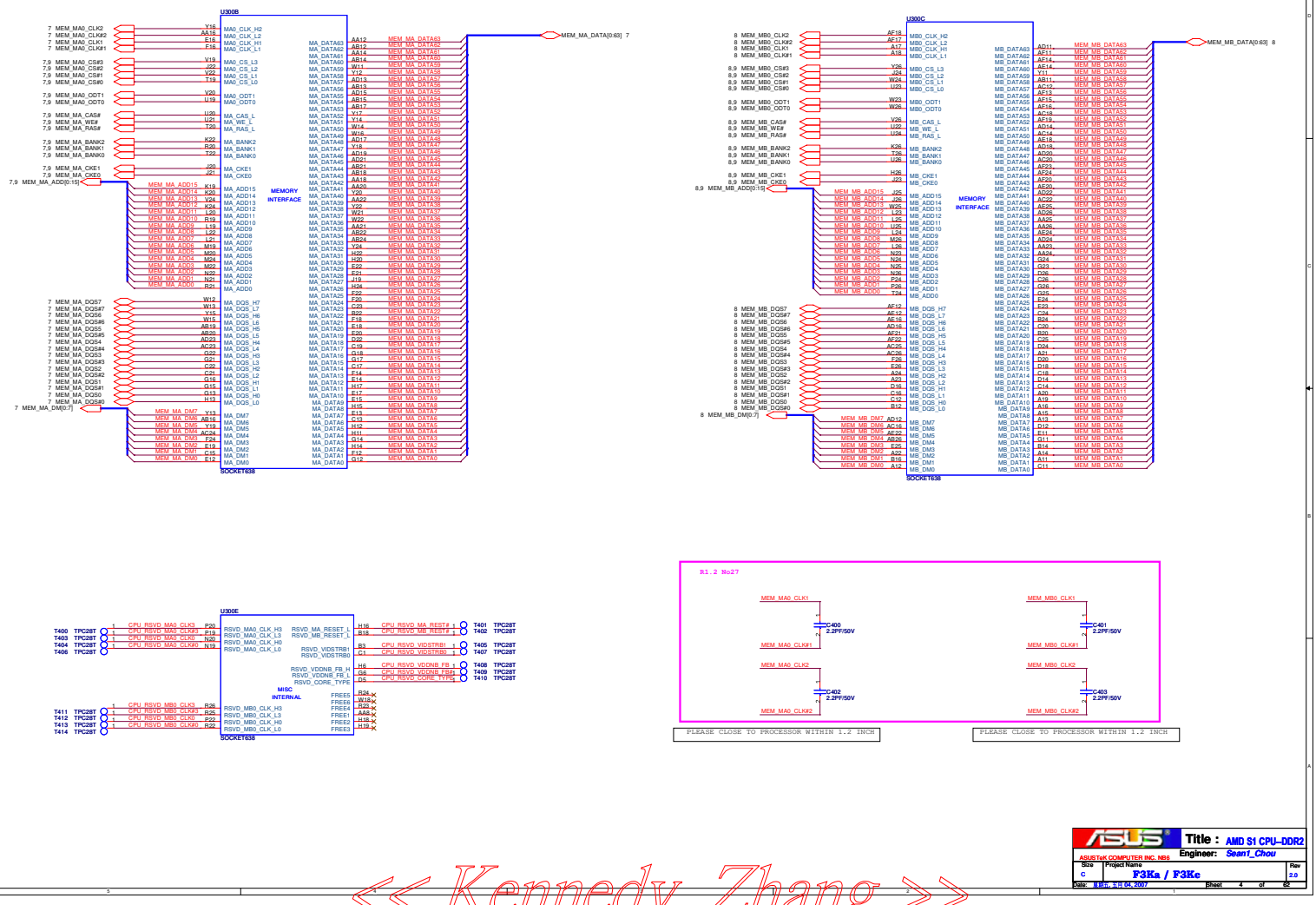
Engineer: Sean1_Chou

Size	Project Name	Rev
Custom	F3Ka / F3Ke	2.0

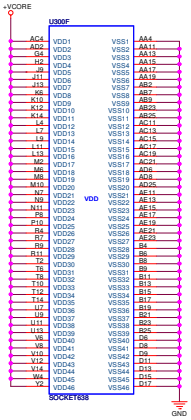
Date: 星期六, 五月 04, 2007 Sheet 1 of 51

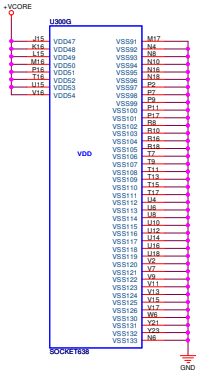


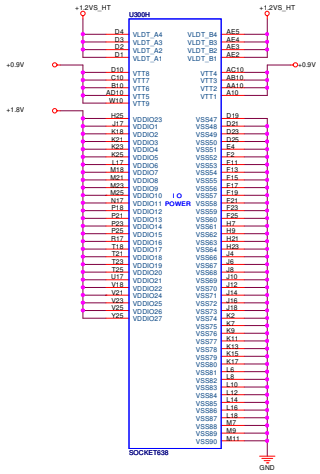
ASUSTeK COMPUTER INC. NB6	Title : AMD S1 CPU-HT		
	Engineer: Sean1_Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: Wednesday, April 04, 2007	Sheet 3 of 62		

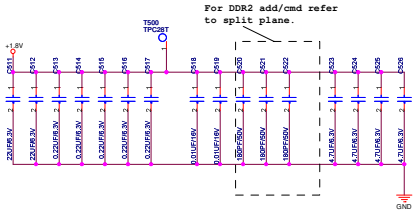


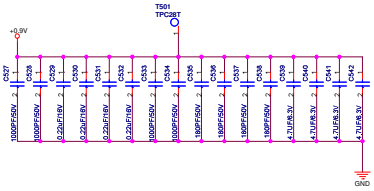
ASUSTeK COMPUTER INC. NB6	Title : AMD S1 CPU-DDR2		
	Engineer: Sean1_Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: Wed, Jul 04, 2007	Sheet 4 of 62		

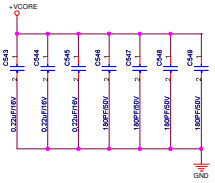


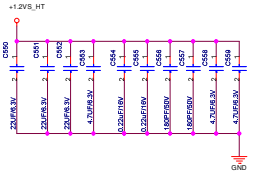






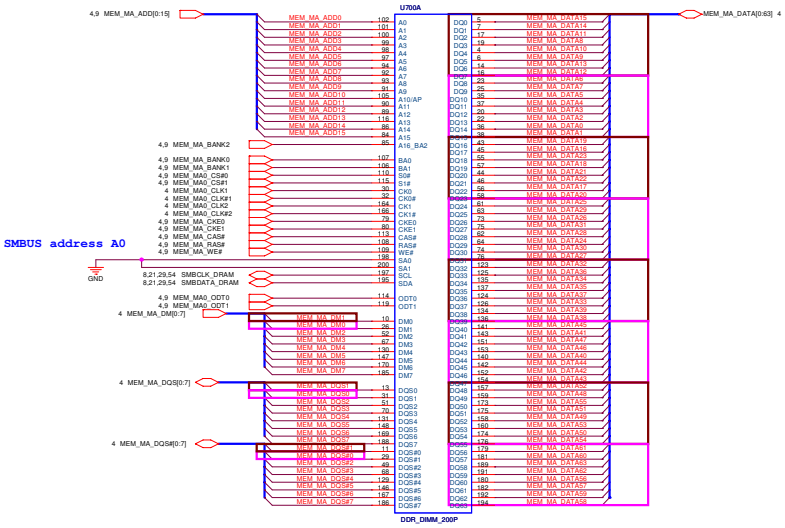


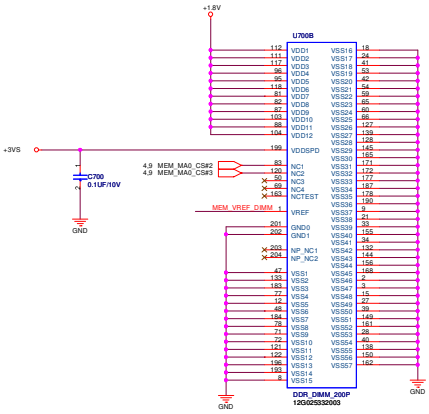




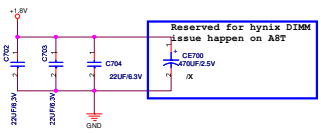
ASUSTECH	Title : AMD S1 CPU(3)-PWR/GND		
	Engineer: Sean1 Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: 星期二, 五月 04, 2007	Sheet 5 of 52		

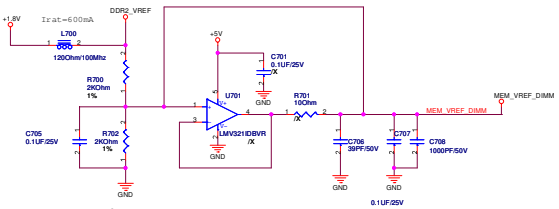
REV . TYPE





Main source is 12G025332003.(FOXCONN)
Second source is 12G025122006.(TYCO)



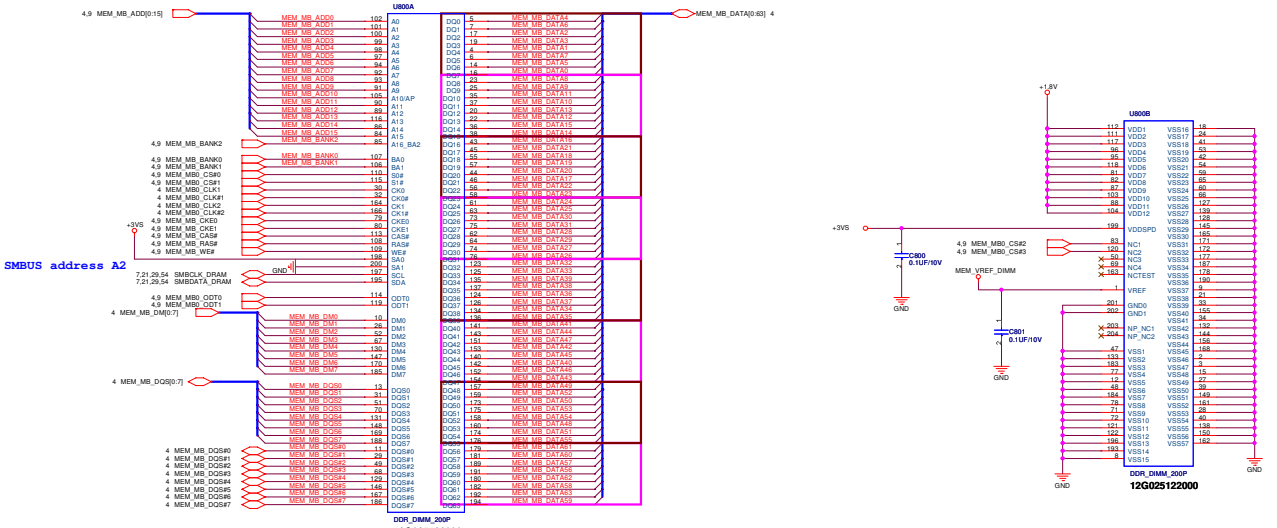


Nearby SO-DIMM

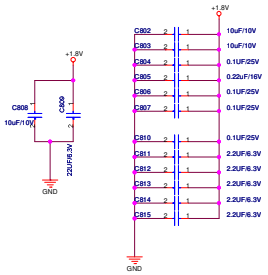
ASUSTECH	Title : DDR2_SO_DIMM-1		
	Engineer: Sean1_Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: 星期, 五 04, 2007	Sheet 7 of 82		

<< Kennedy_Zhang >>

STD. TYPE

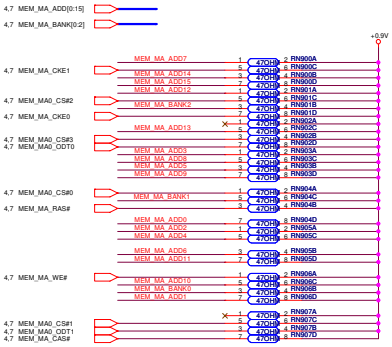


Main source is 12G025122000.(FOXCONN)
Second source is 12G025122007.(TYCO)

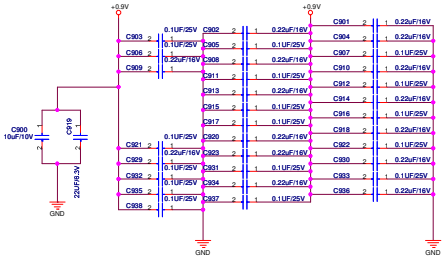


ASUSTECH	Title : DDR2_SO_DIMM-2	
	Engineer: Sean1_Chou	
Size: C	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期二, 8 月 04, 2007	Sheet 8 of 82	

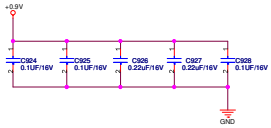
<< Kennedy_Zhang >>



Layout Note: Place one cap close to every 2 pullup resitors terminated to +0.9V

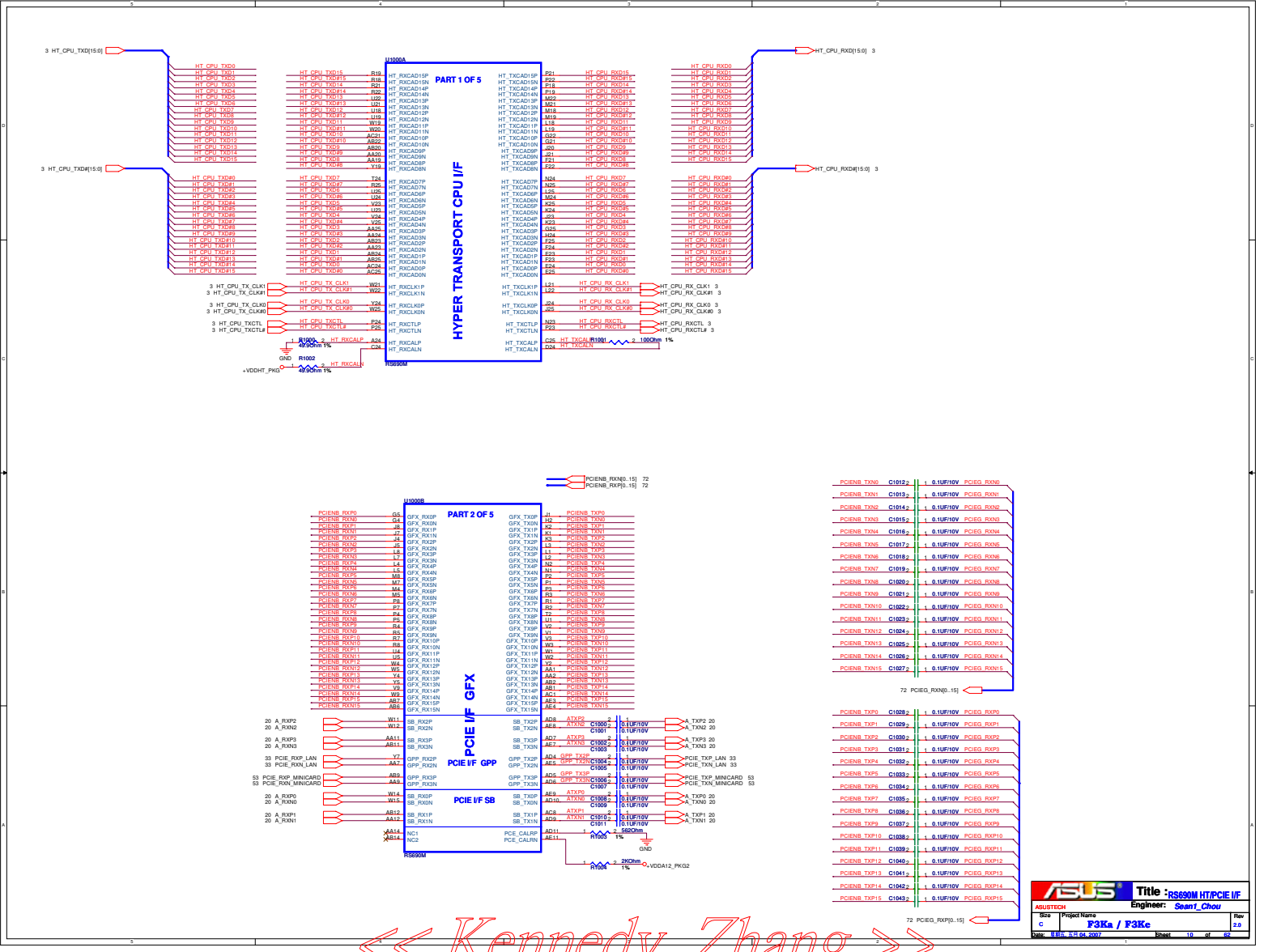


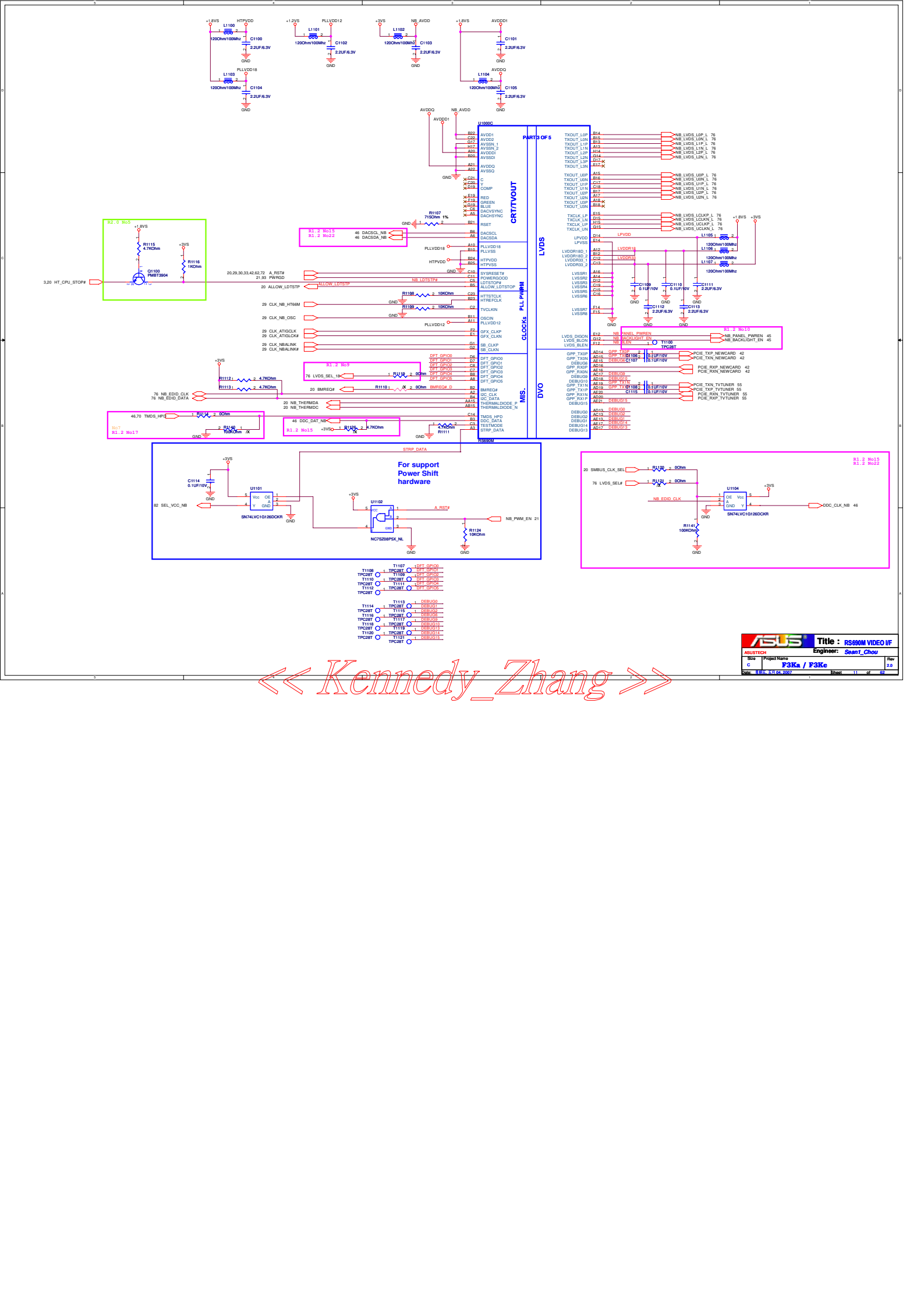
Near to +0.9V array resistors.

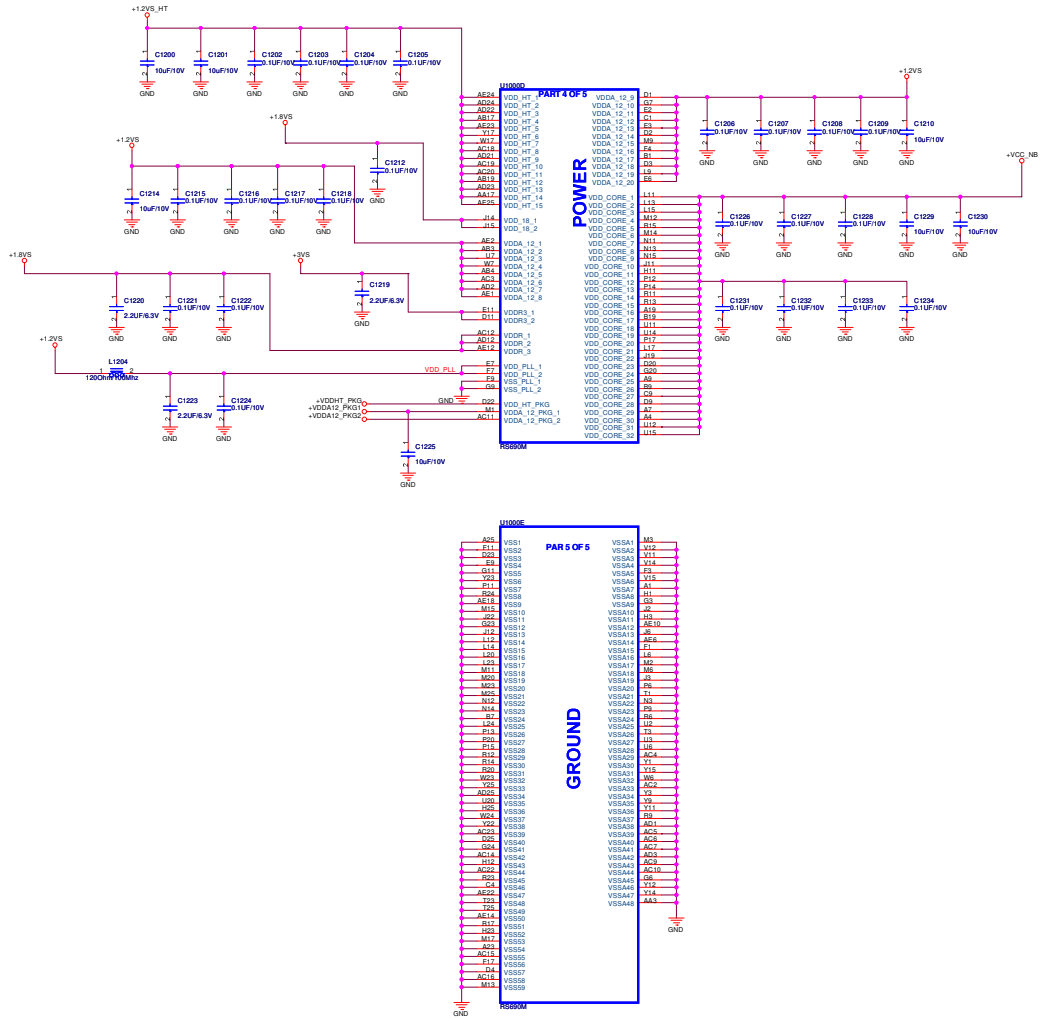


ASUSTeK	Title : DDR2_SODIMMS TERM	
	Engineer: Sean1_Chou	
Size: C	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期二, 8 月 04, 2007	Sheet 9 of 52	

<< Kennedy_Zhang >>

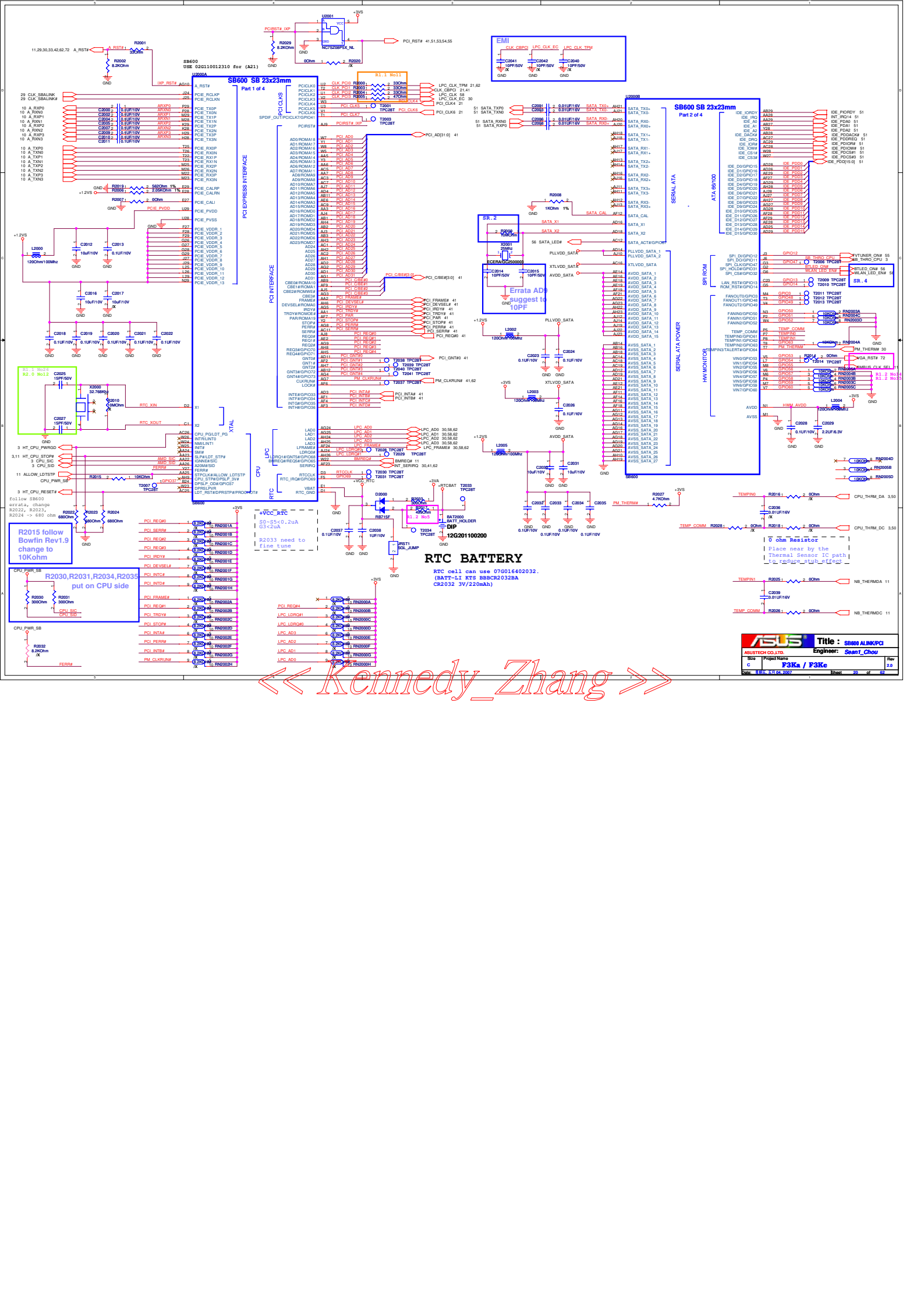


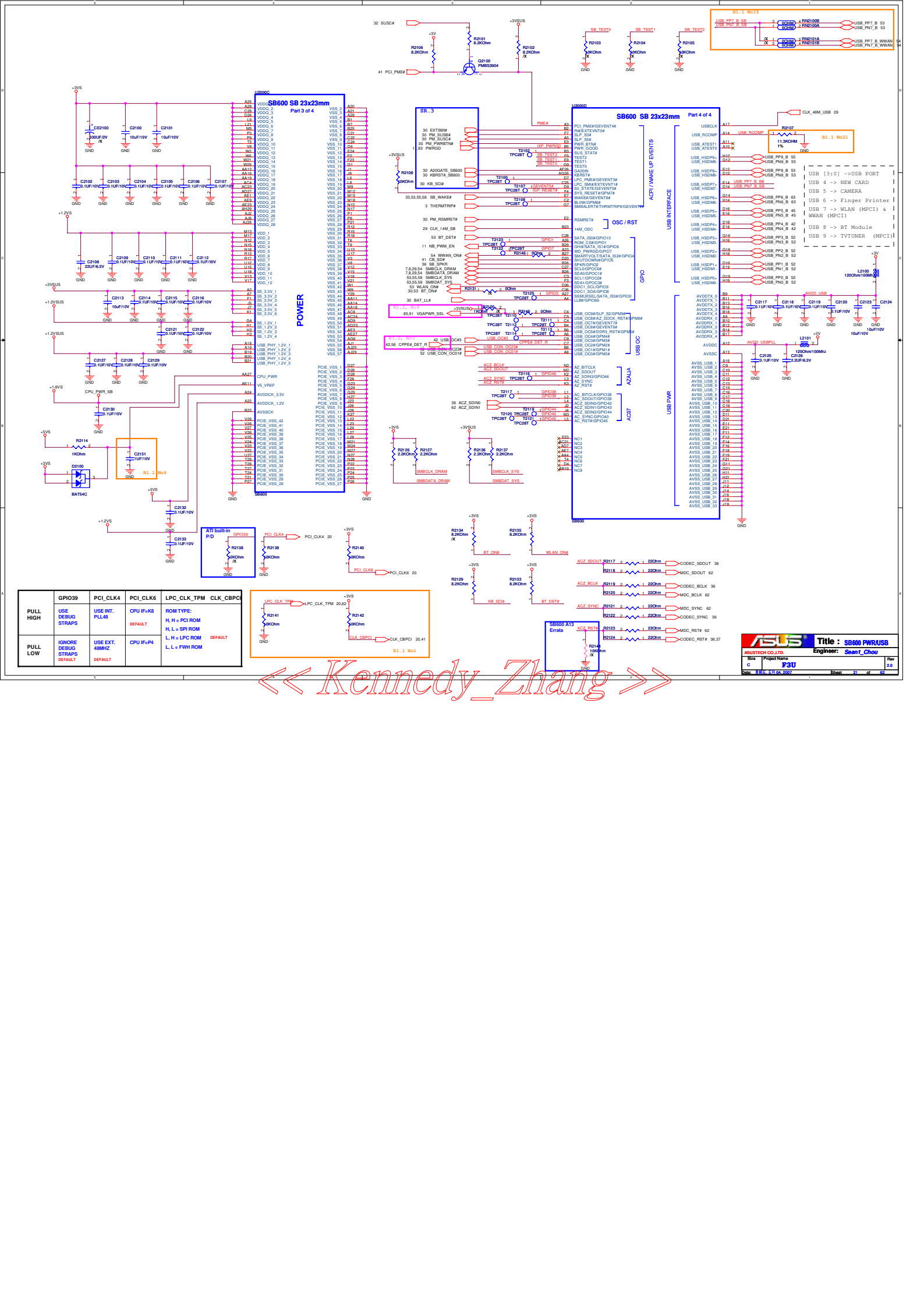




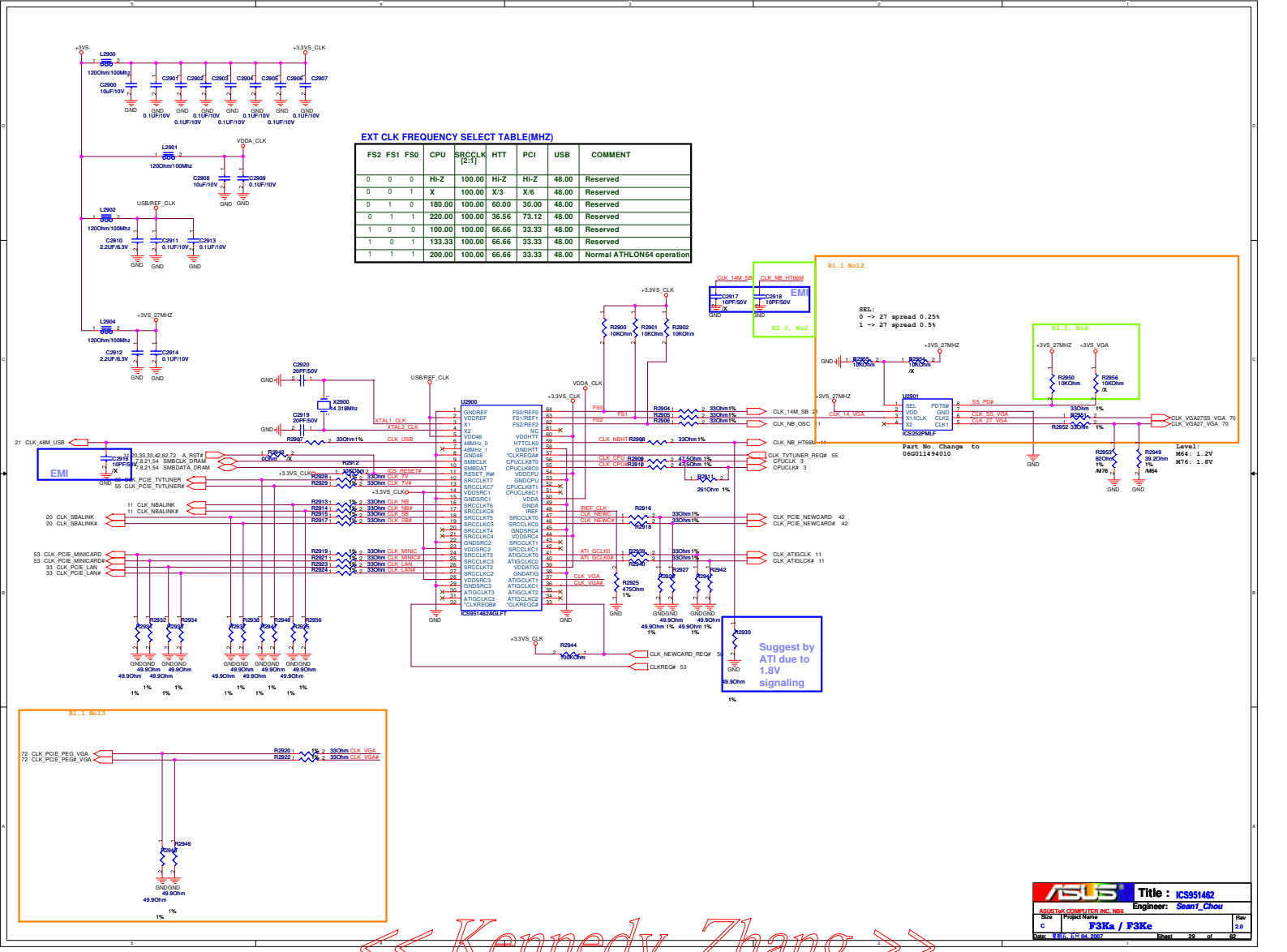
ASUSTECH	Title : RS690M PWR		
	Engineer: Sean1_Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: 星期二, 五月 04, 2007	Sheet 12 of 52		

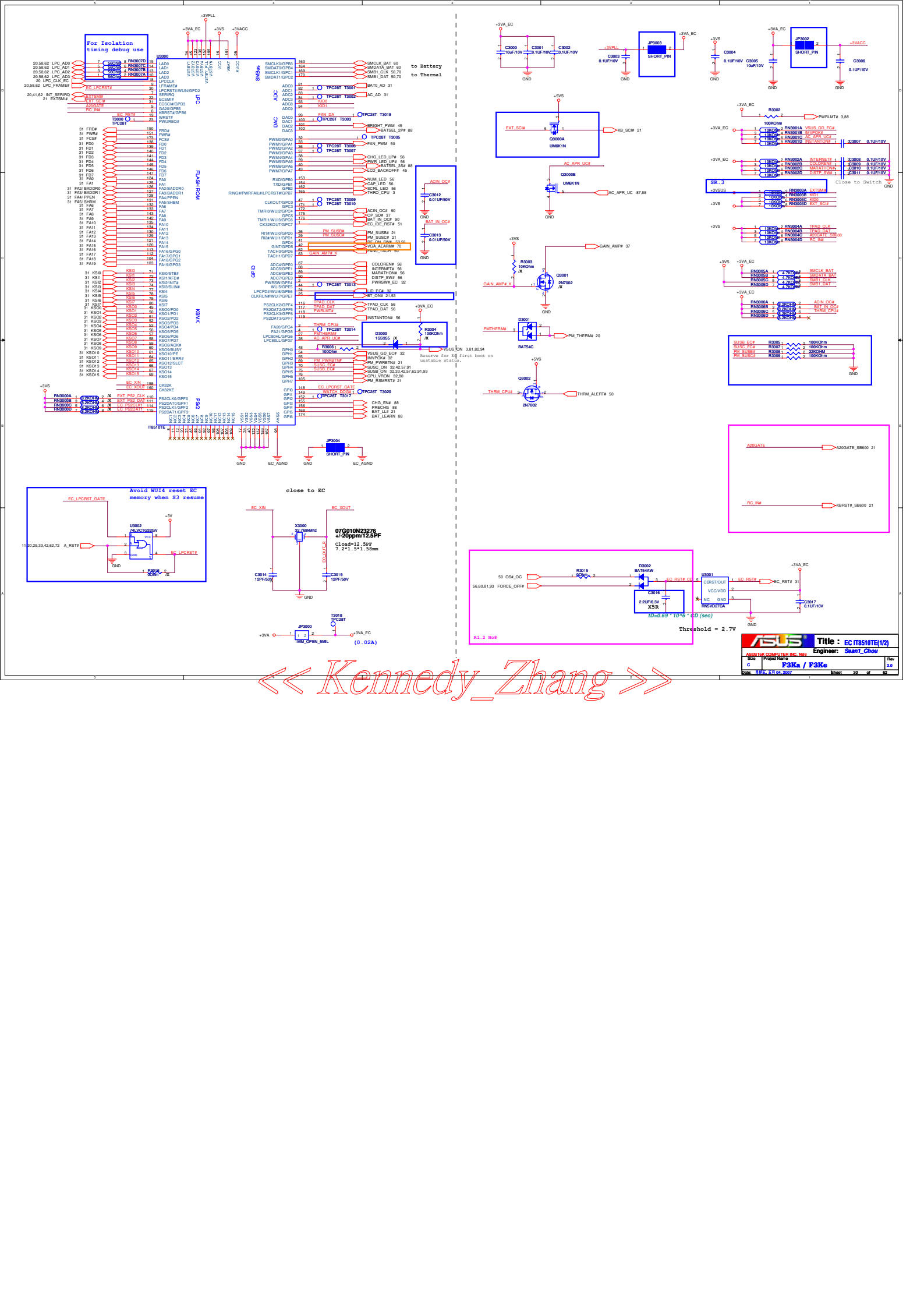
<< Kennedy_Zhang >>


SB600
USE 02G110012310 for (A21)
SB600 SB 23x23mm
Part 1 of 4
SB600 SB 23x23mm
Part 2 of 4
EMI
PCI EXPRESS INTERFACE
PCI INTERFACE
SERIAL ATA
SERIAL ATA POWER
ATA 66*100
SPI ROM
HW MONITOR
XTAL
LPC
CPU
RTC
R2015 follow Bowfin Rev1.9 change to 10Kohm
R2030,R2031,R2034,R2035 put on CPU side
R2033 need to fine tune
0 ohm Resistor
Place near by the Thermal Sensor IC path to reduce stub effect
RTC BATTERY
RTC cell can use 07G016402032.
(BATT-LI KTS BBBCR2032BA
CR2032 3V/220mAh)
Errata AD9 suggest to 10PF
Title : SB600 ALINK/PCI
Engineer: Sean1_Chou
ASUSTeK CO.,LTD.
F3Ka / F3Ke
Date: 星期二, 8 月 04, 2007
Sheet 20 of 82
<< Kennedy_Zhang >>

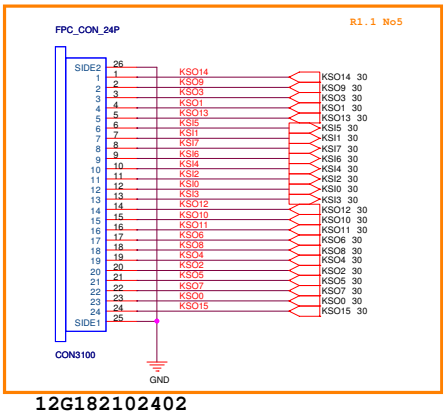


	GPIO39	PCI_CLK4	PCI_CLK6	LPC_CLK_TPM	CLK_CBPCI
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

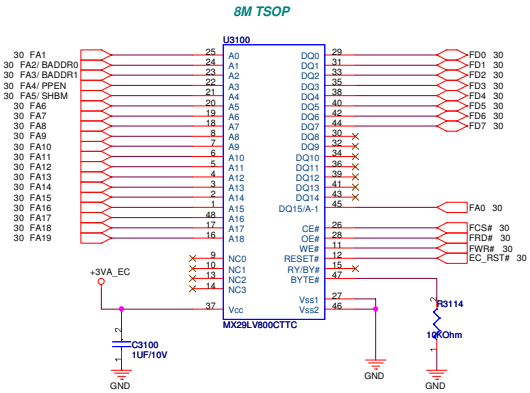



For Isolation timing debug use
U3000
IT8510TE
to Battery
to Thermal
close to EC
Avoid WUI4 reset EC memory when S3 resume
07G010N23276
+/-20ppm/12.5PF
Cload=12.5PF
7.2*1.5*1.58mm
ID=0.69 * 10^6 * CD (sec)
Threshold = 2.7V
(0.02A)
Close to Switch
Reserve for EC first boot on unstable status.
Title : EC IT8510TE(1/2)
Engineer: Sean1_Chou
ASUSTeK COMPUTER INC. NB8
F3Ka / F3Ke
Date: 日期, 8 04, 2007
Sheet 30 of 62
<< Kennedy_Zhang >>

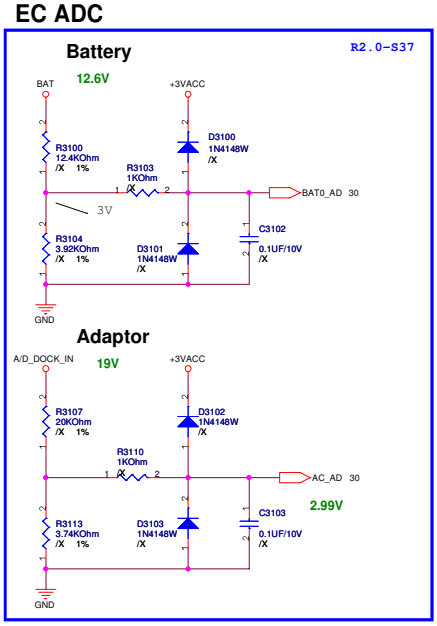
KBC connector



12G182102402

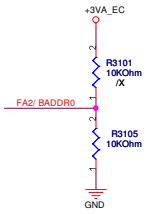


EC ADC

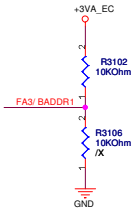


EC Hardware Strap

strap value sampled after VSTBY power up reset

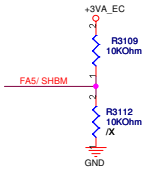


PNPCFG base address set by SWCBAHR/SWCBALR

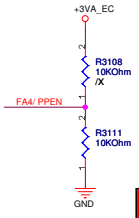


BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

Share Memory

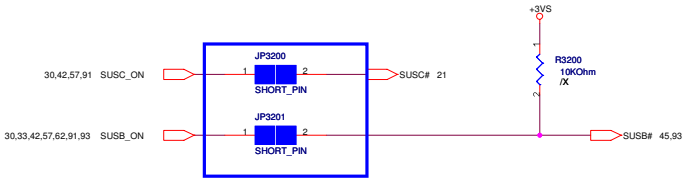


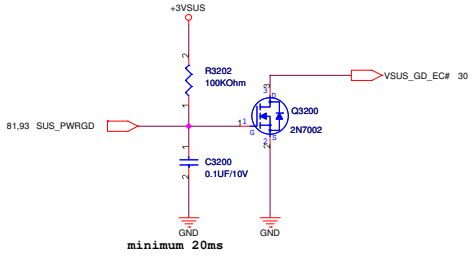
SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

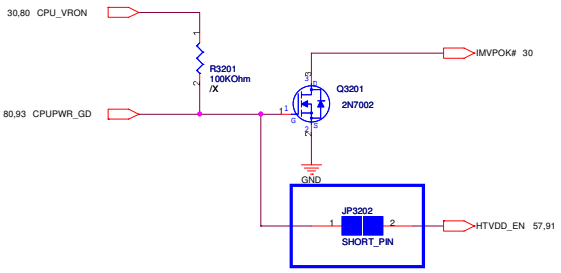


PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

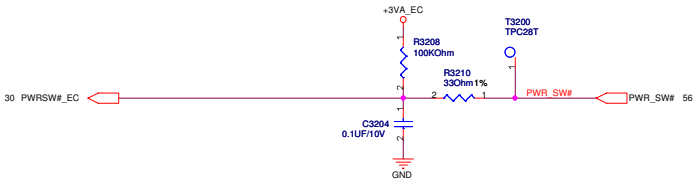
ASUSTeK COMPUTER INC. NB6	Title : EC IT8510TC(2/2)	
	Engineer: Sean1_Chou	
Size: Custom	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 31 of 62	



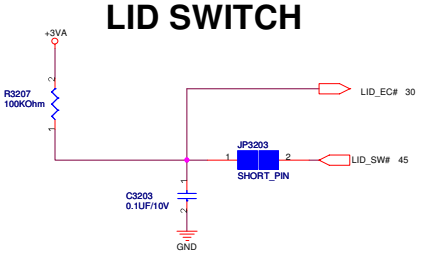




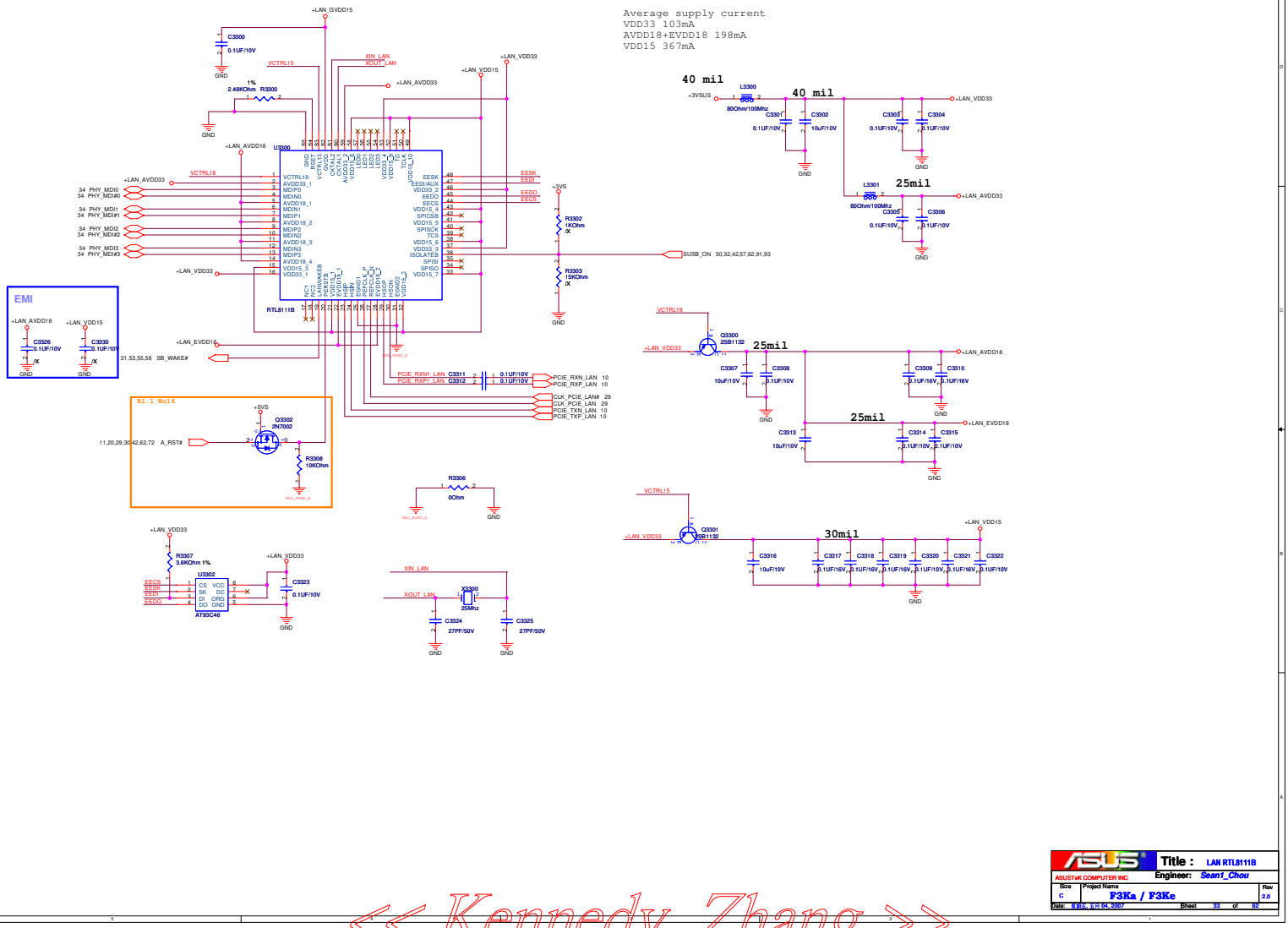
POWER SWITCH



LID SWITCH

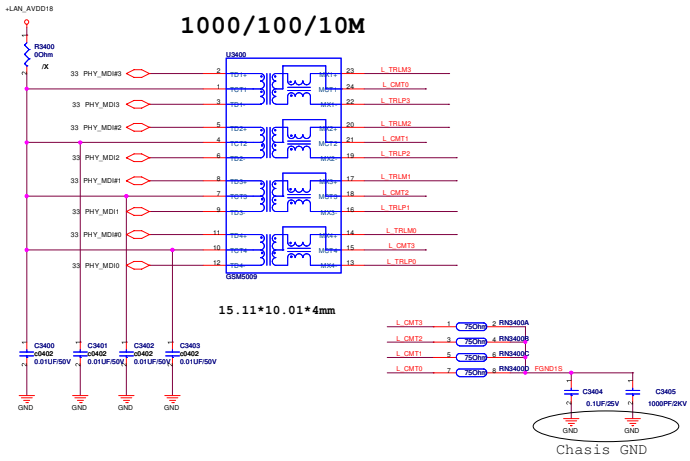


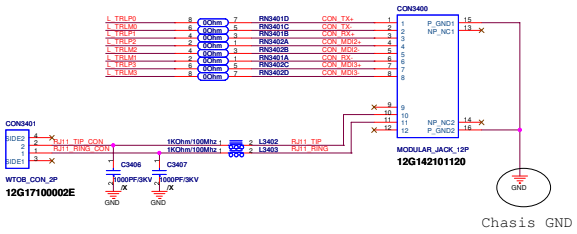
ASUSTeK COMPUTER INC	Title : POWER-ON SEQUENCE	
	Engineer: Sean1_Chou	
Size: Custom	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 32 of 62	



<< Kennedy_Zhang >>

LAN PORT





ASUSTeK COMPUTER INC

Title: RJ11&RJ45 CONNECTOR

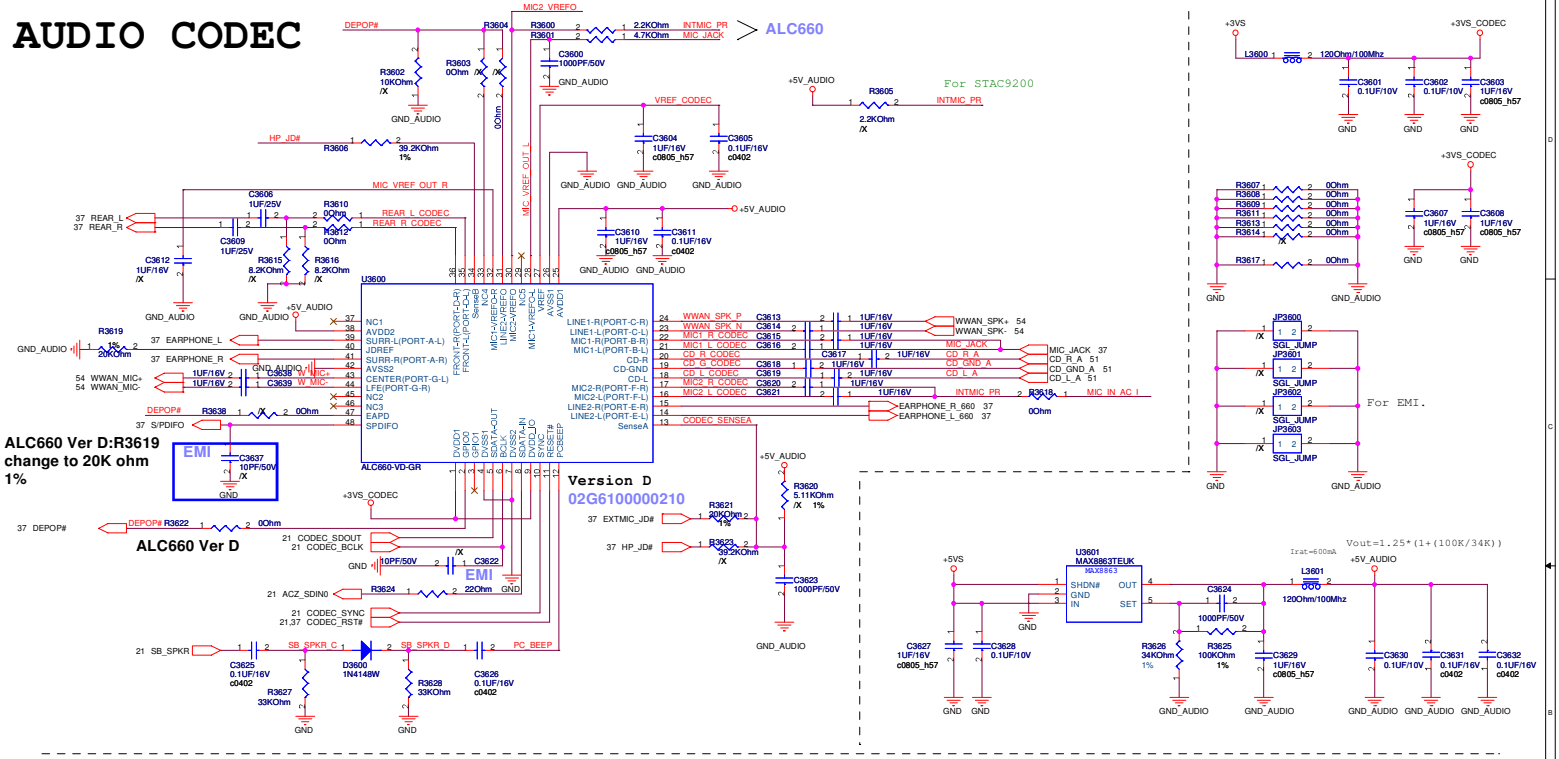
Engineer: Sean1_Chou

Size	Project Name	Rev
C	F3Ka / F3Ke	2.0

Date: Mon, Jul 04, 2007 Sheet 34 of 62

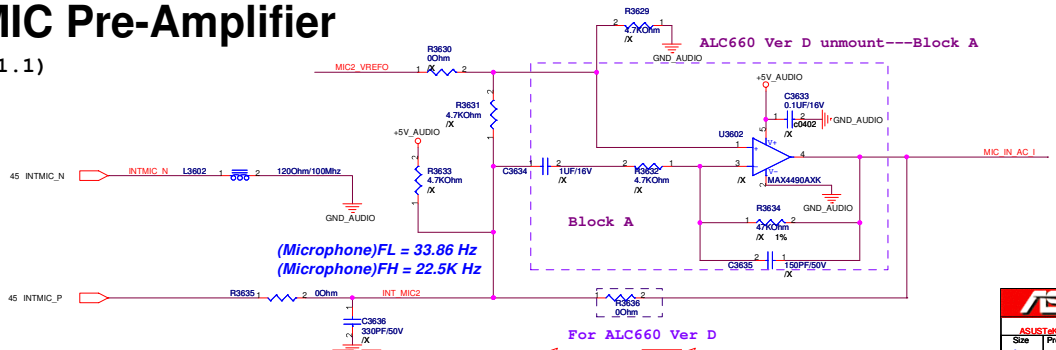
<< Kennedy_Zhang >>

AUDIO CODEC



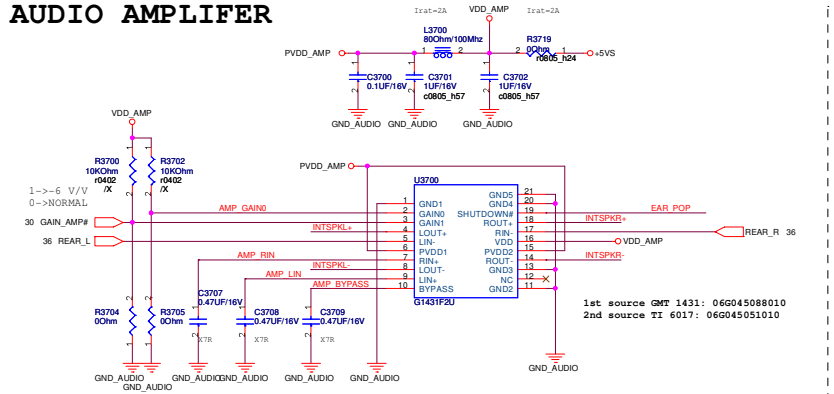
Internal MIC Pre-Amplifier

(Follow F2J R1.1)

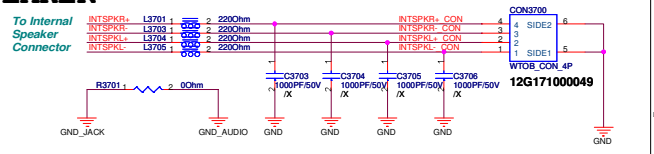


Title :	AUDIO CODEC-ALC660
ASUSTeK COMPUTER INC.	Engineer: Sean1_Chou
Size: Custom	Project Name: F3Ka / F3Ke
Rev: 2.0	
Date: 星期六, 六月 04, 2007	Sheet 36 of 62

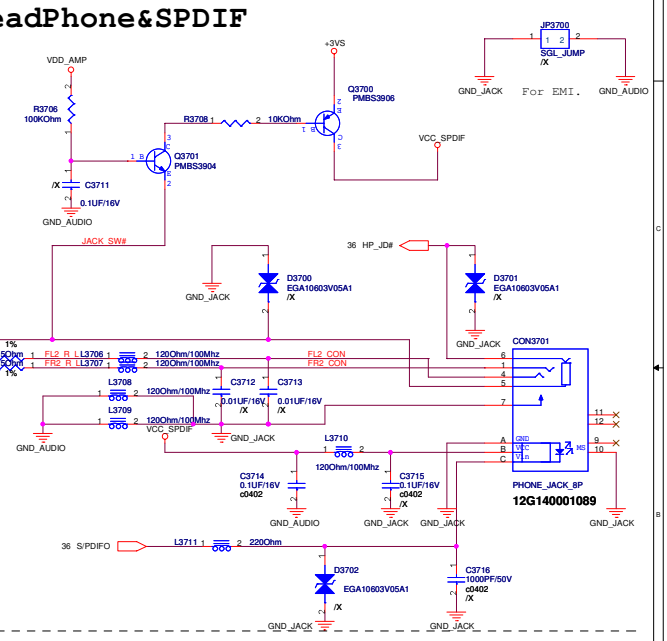
AUDIO AMPLIFER



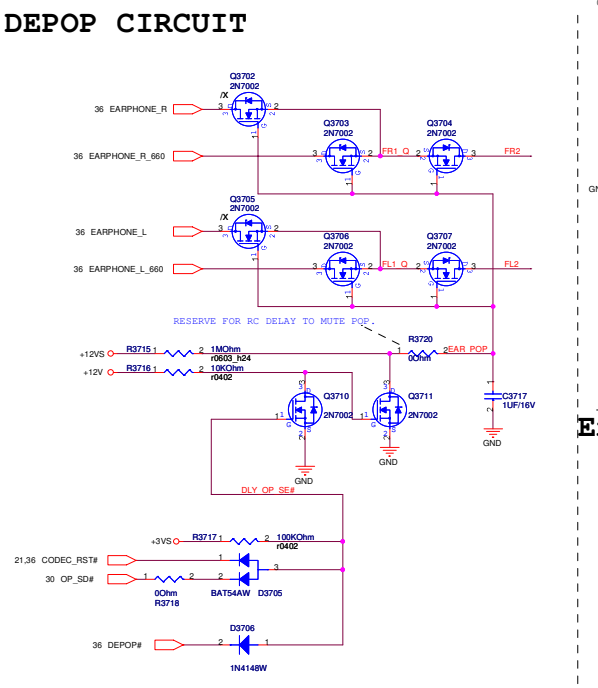
SPEAKER



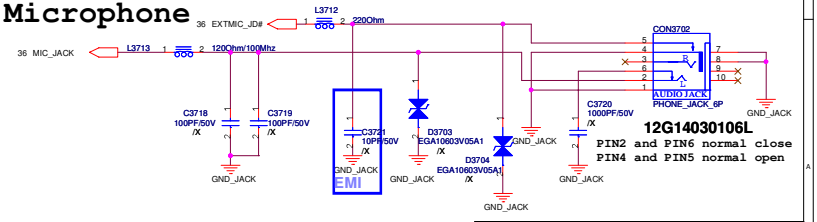
HeadPhone&SPDIF



DEPOP CIRCUIT



External Microphone



ASUSTeK COMPUTER INC.

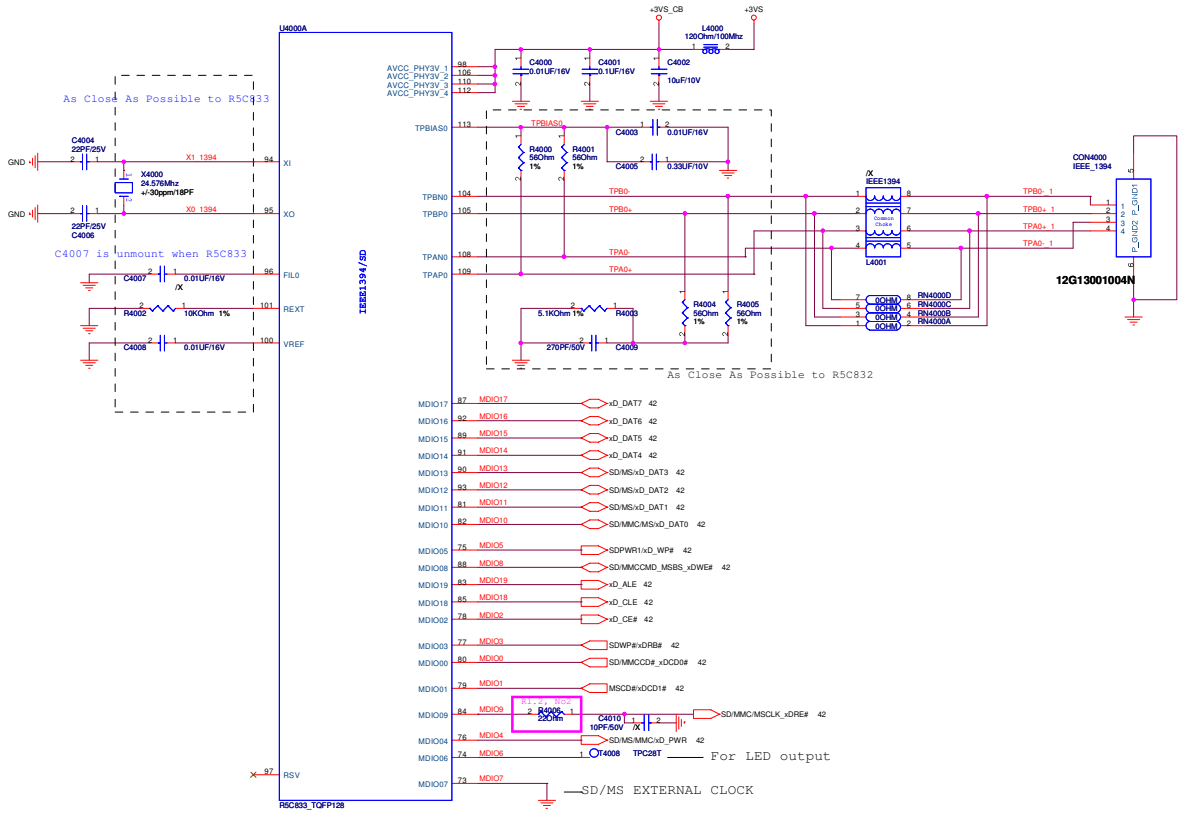
Title : AUDIO AMP & JACK

Engineer: Sean1_Chou

Size	Project Name	Rev
Custom	F3Ka / F3Ke	2.0

Date: 星期六, 六月 04, 2007 Sheet 37 of 62

<< Kennedy_Zhang >>



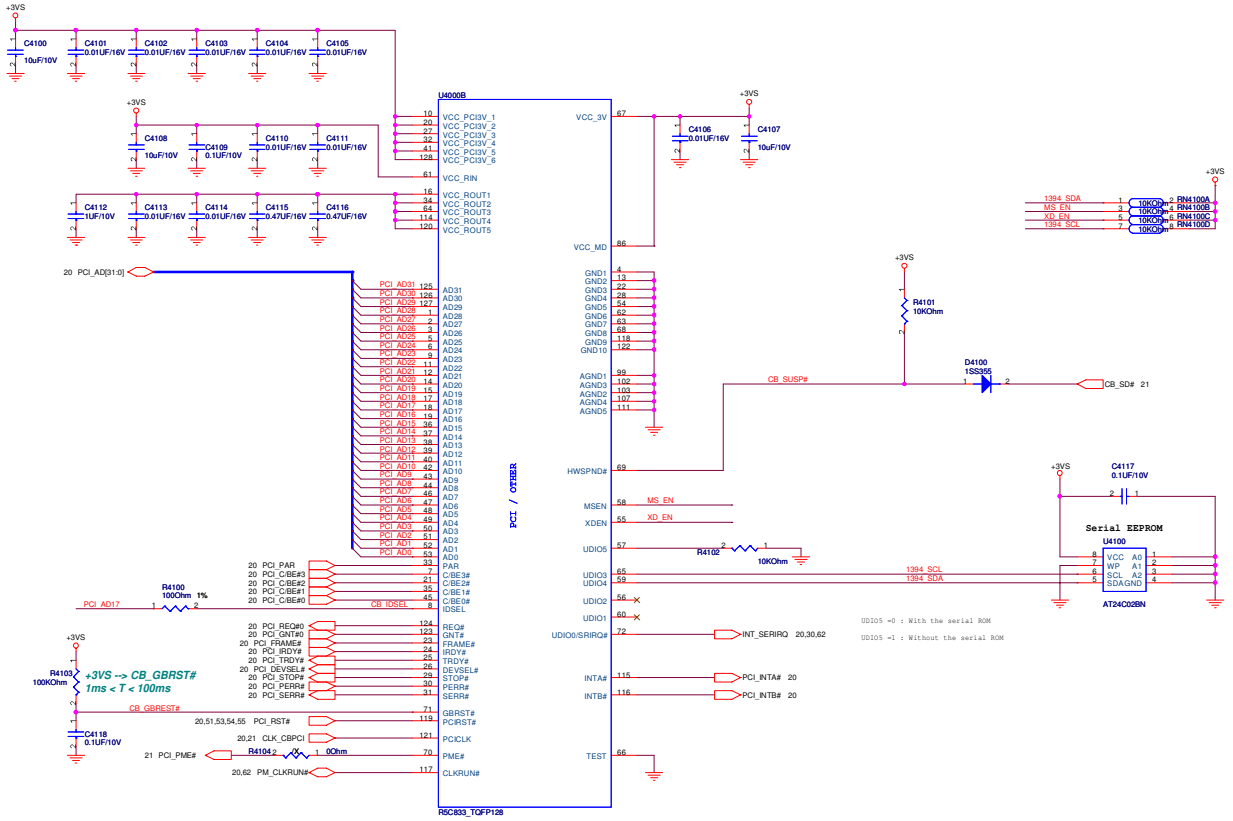

```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```

```
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO07--> SD External Clock/
          MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

ASUSTek COMPUTER INC	Title : RICOH 5C832-CARD&1394		
	Engineer: Sean1_Chou		
Size: Custom	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 40 of 62		

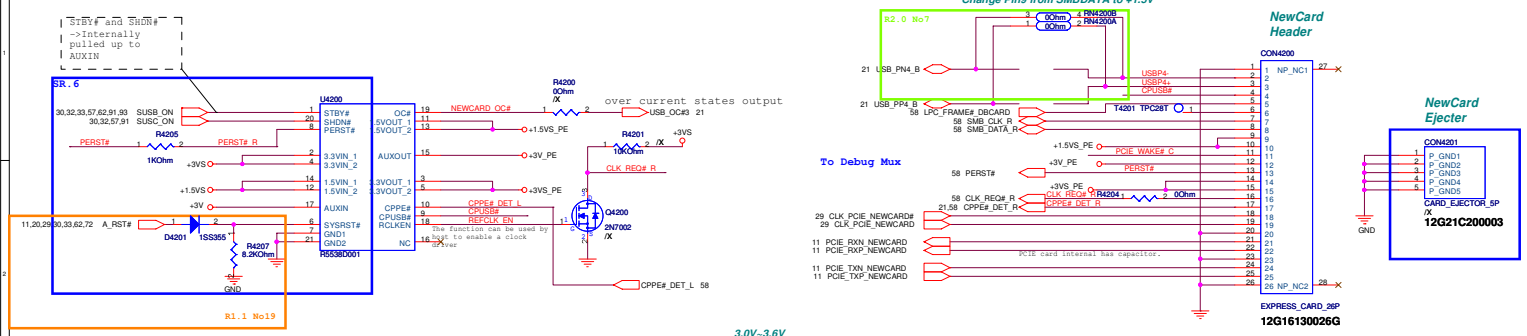
<< Kennedy_Zhang >>

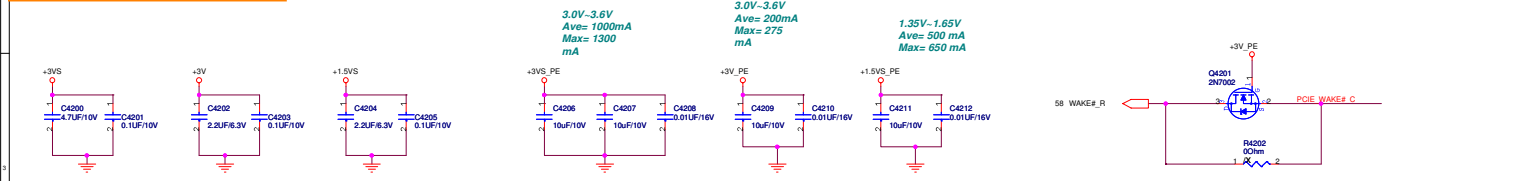


ASUSTeK COMPUTER INC	Title : RICOH 5C832-PCI	
	Engineer: Sean1_Chou	
Size: Custom	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 41 of 62	

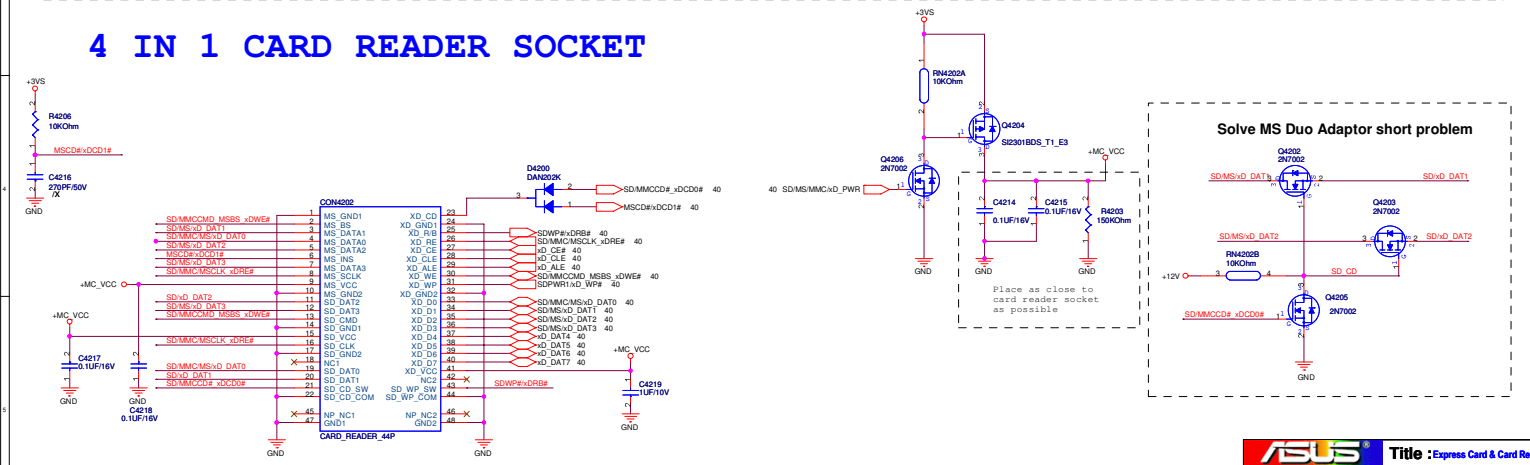
NEW CARD SOCKET

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V





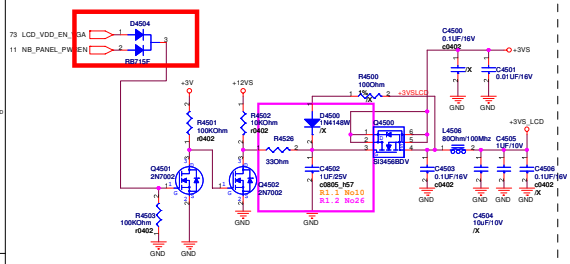
4 IN 1 CARD READER SOCKET



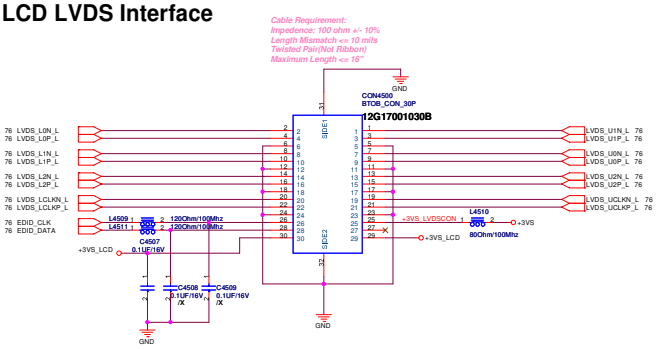
ASUS	Title : Express Card & Card Reader		
ASUSTeK COMPUTER INC. NB6	Engineer: Sean1_Chou		
Size: Custom	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 42 of 62		

<< Kennedy_Zhang >>

LCD Power

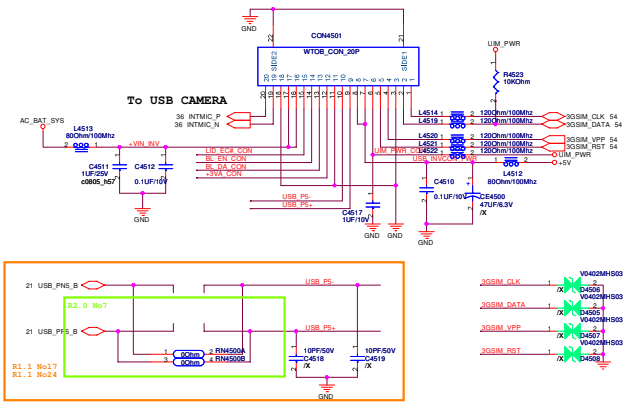


LCD LVDS Interface



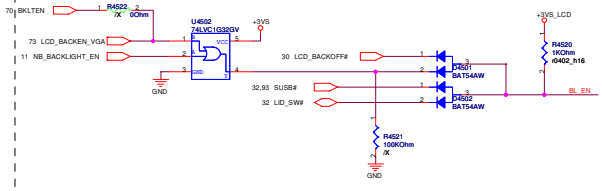
INVERTER Interface

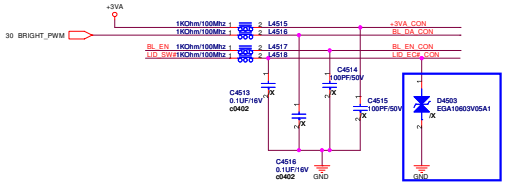
12G171000201



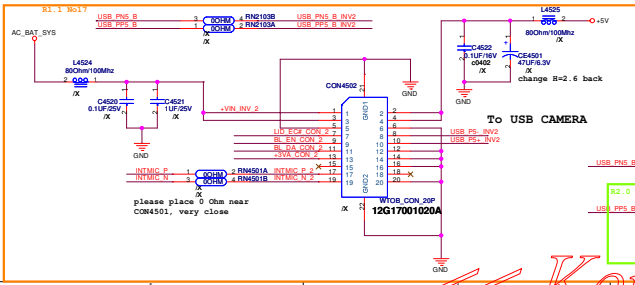
Backlight Enable

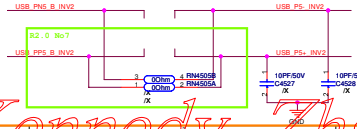
BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.





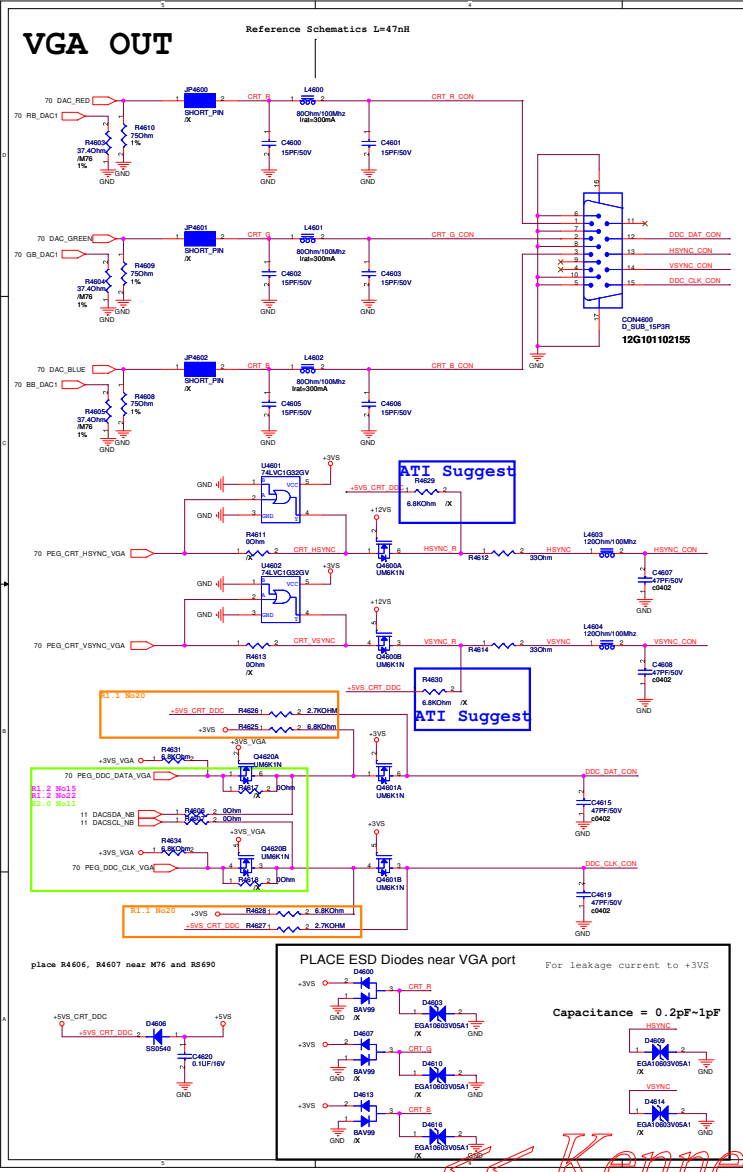
USB5 colay for INV1 and INV2





ASUSTECH	Title : LVDS & INVERTER CONNECTOR	
	Engineer: Sean1_Chou	
Size: C	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: Fri, 04, 2007	Sheet 45 of 62	

VGA OUT



DVI-D

TV OUT

ASUSTeK

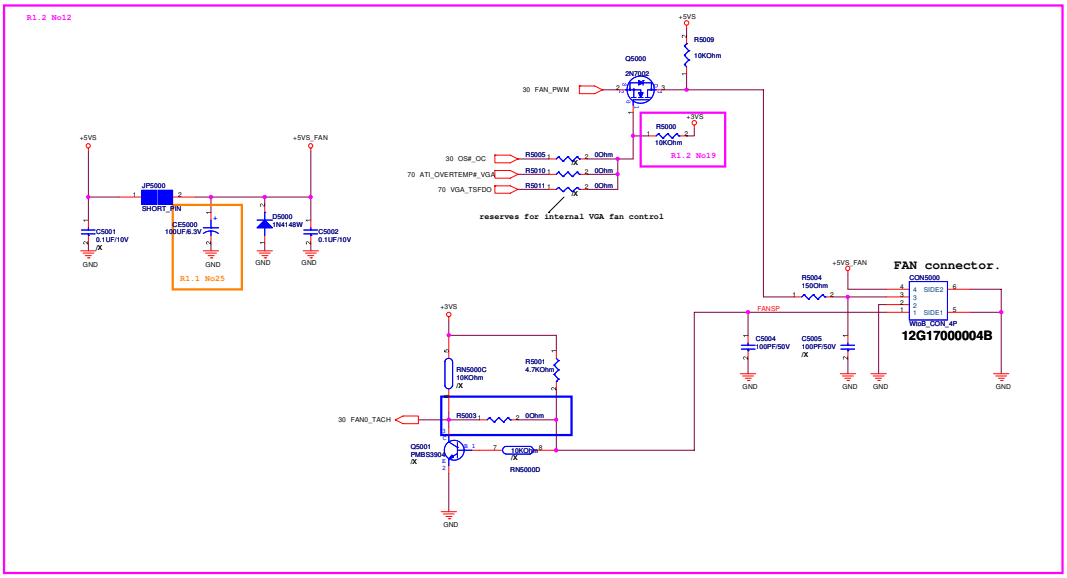
Title : TV&CRT CONNECTOR

Engineer: Sean1_Chou

Size	Project Name	Rev
C	F3Ka / F3Ke	2.0

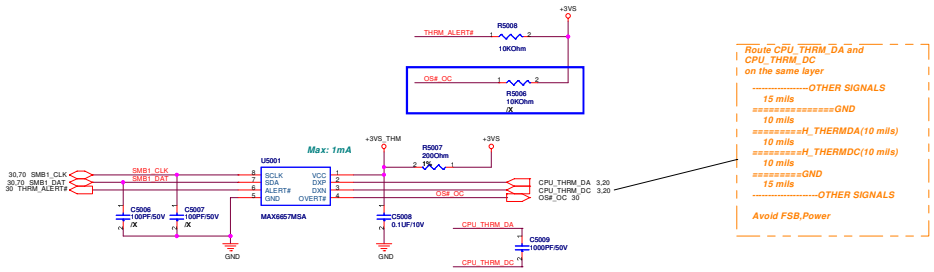
Date: 星期二, 8 月 04, 2007 Sheet 48 of 82

DC FAN control



CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

Thermal Sensor



Route CPU_THRM_DA and CPU_THRM_DC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

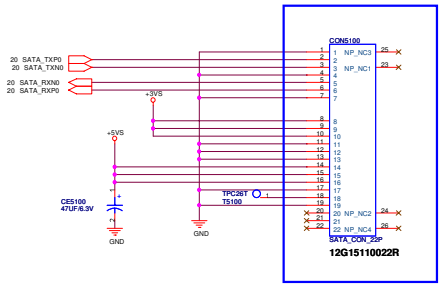
ASUSTeK COMPUTER INC. NB5 — Engineer: Sean1_Chou

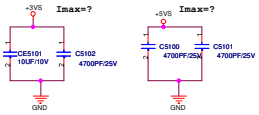
Size	Project Name	Rev
C	F3Ka / F3Ke	2.0

Date: 星期一, 十月 04, 2007 — Sheet 50 of 62

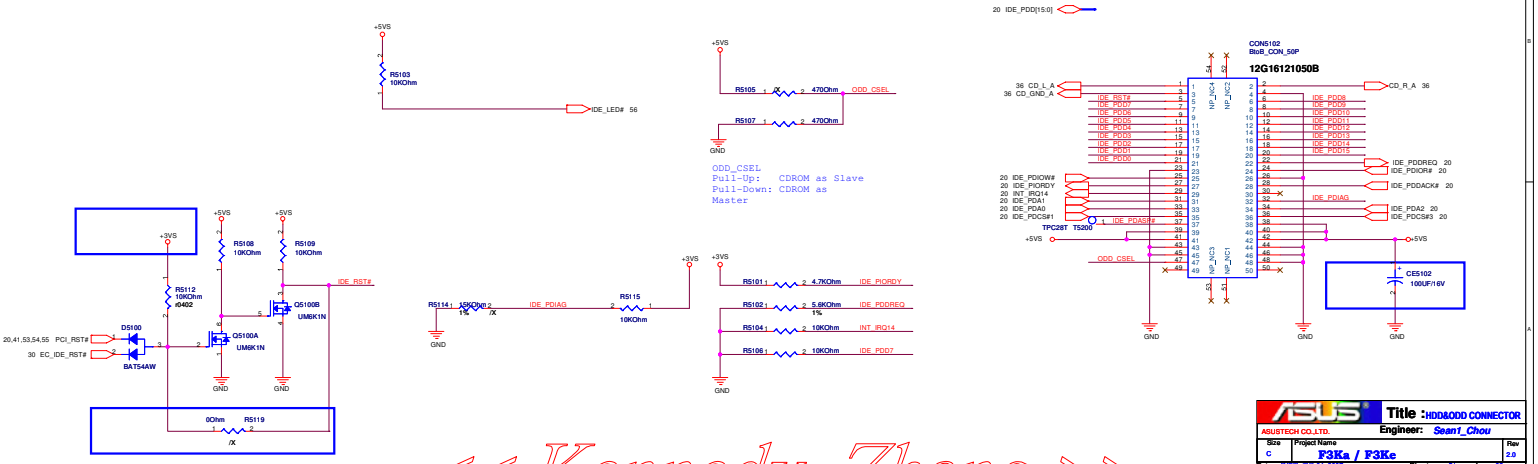
<< Kennedy_Zhang >>

SATA_HDD(Default)





CD-ROM



ASUSTeK COMPUTER INC.

Title : HDD&ODD CONNECTOR

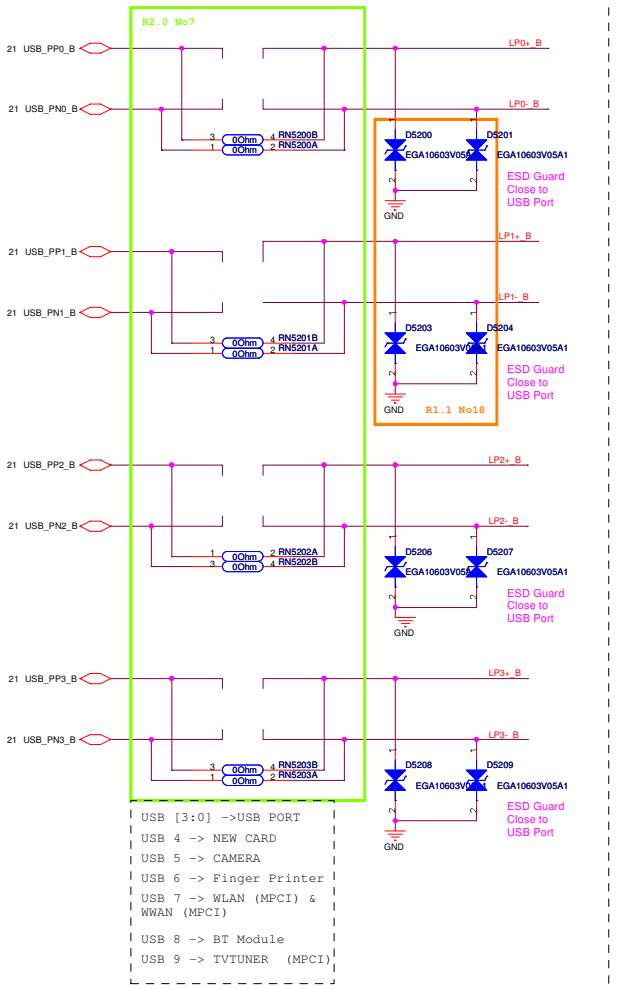
ASUSTECH CO.LTD.

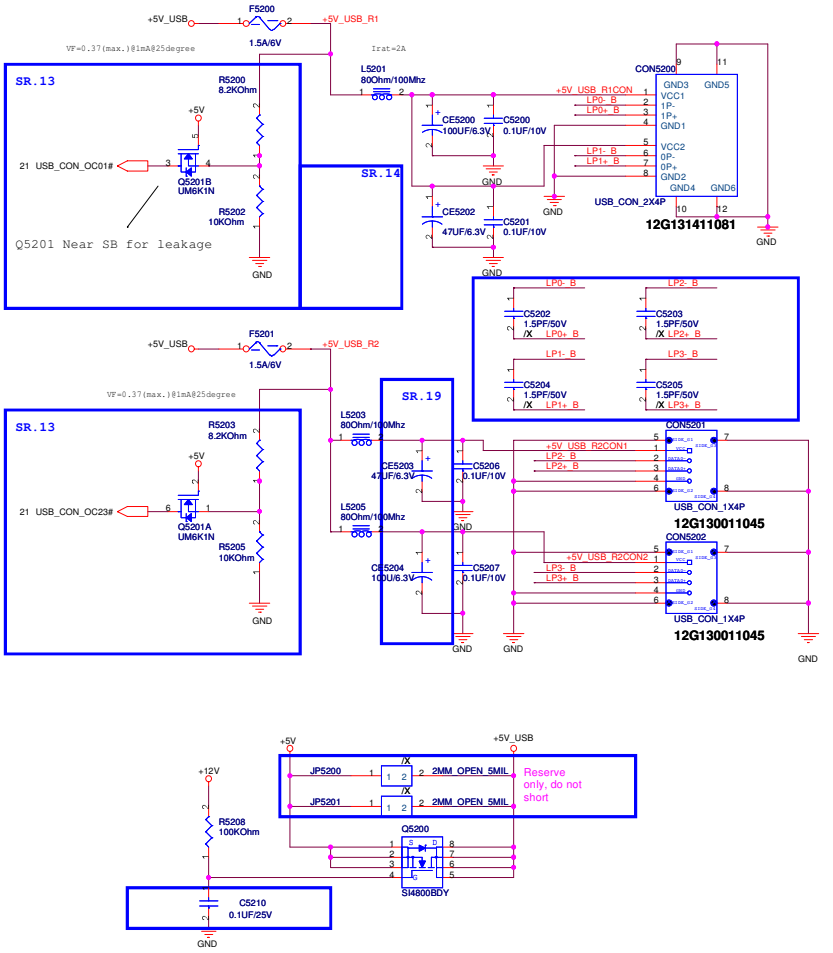
Engineer: Sean1_Chou

Size	Project Name	Rev
C	F3Ka / F3Ke	2.0

Date: Wednesday, March 04, 2007 Sheet 51 of 62

<< Kennedy_Zhang >>



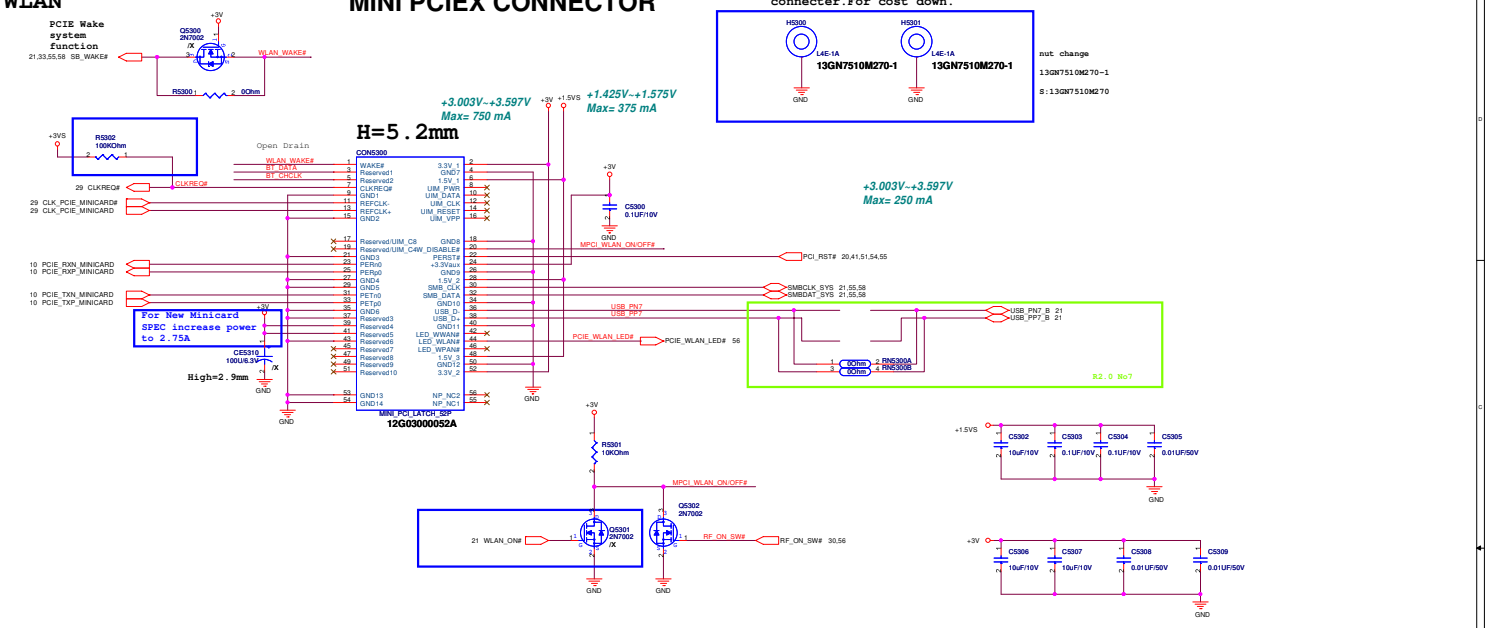


ASUSTeK COMPUTER INC	Title : USB Port x4&USB CAMERA		
	Engineer: Sean1_Chou		
Size: Custom	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 52 of 62		

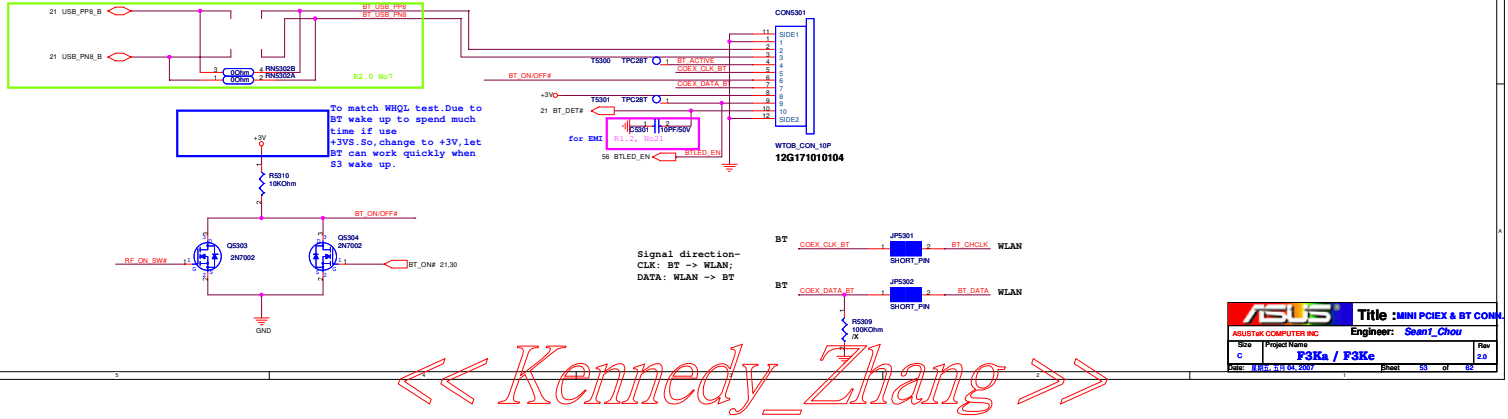
<< Kennedy_Zhang >>

WLAN

MINI PCIEX CONNECTOR

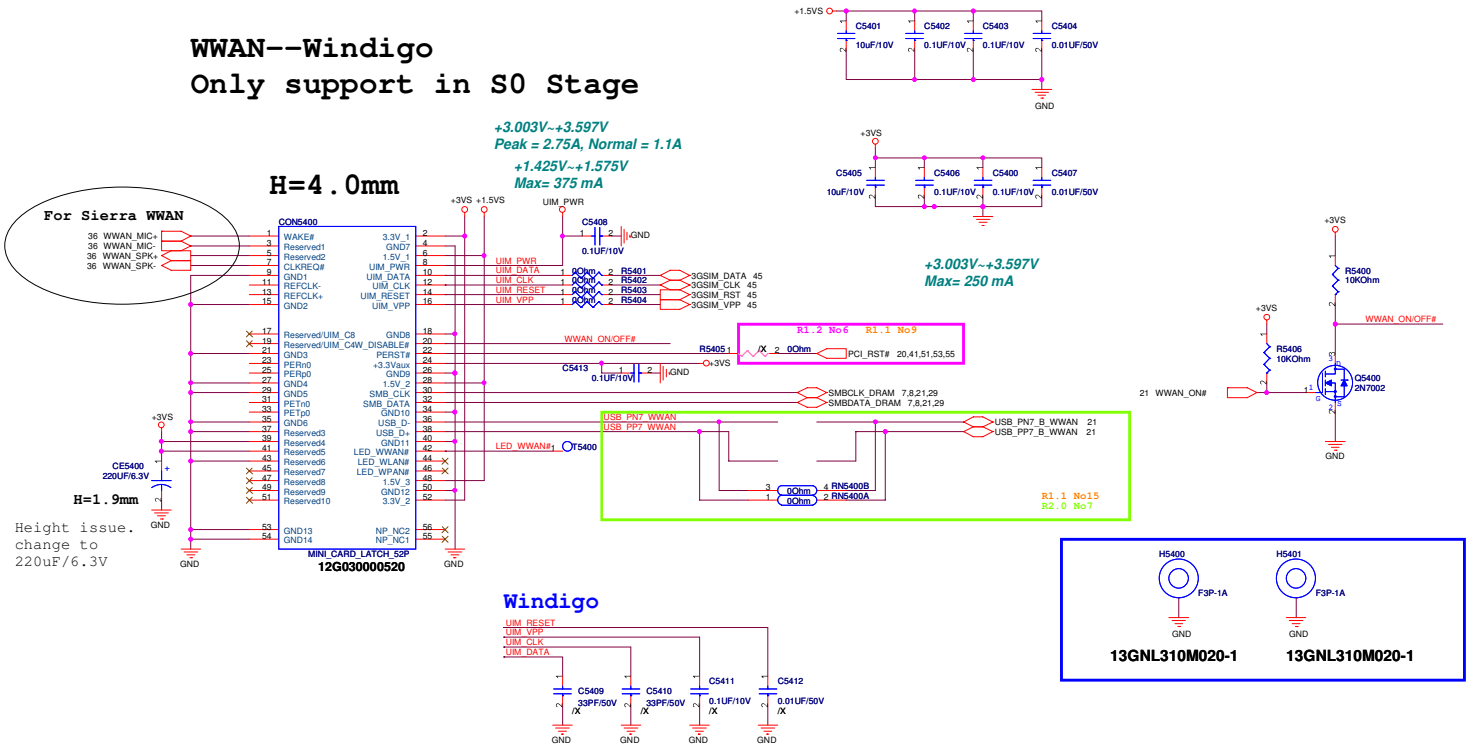


BLUETOOTH CONNECTOR



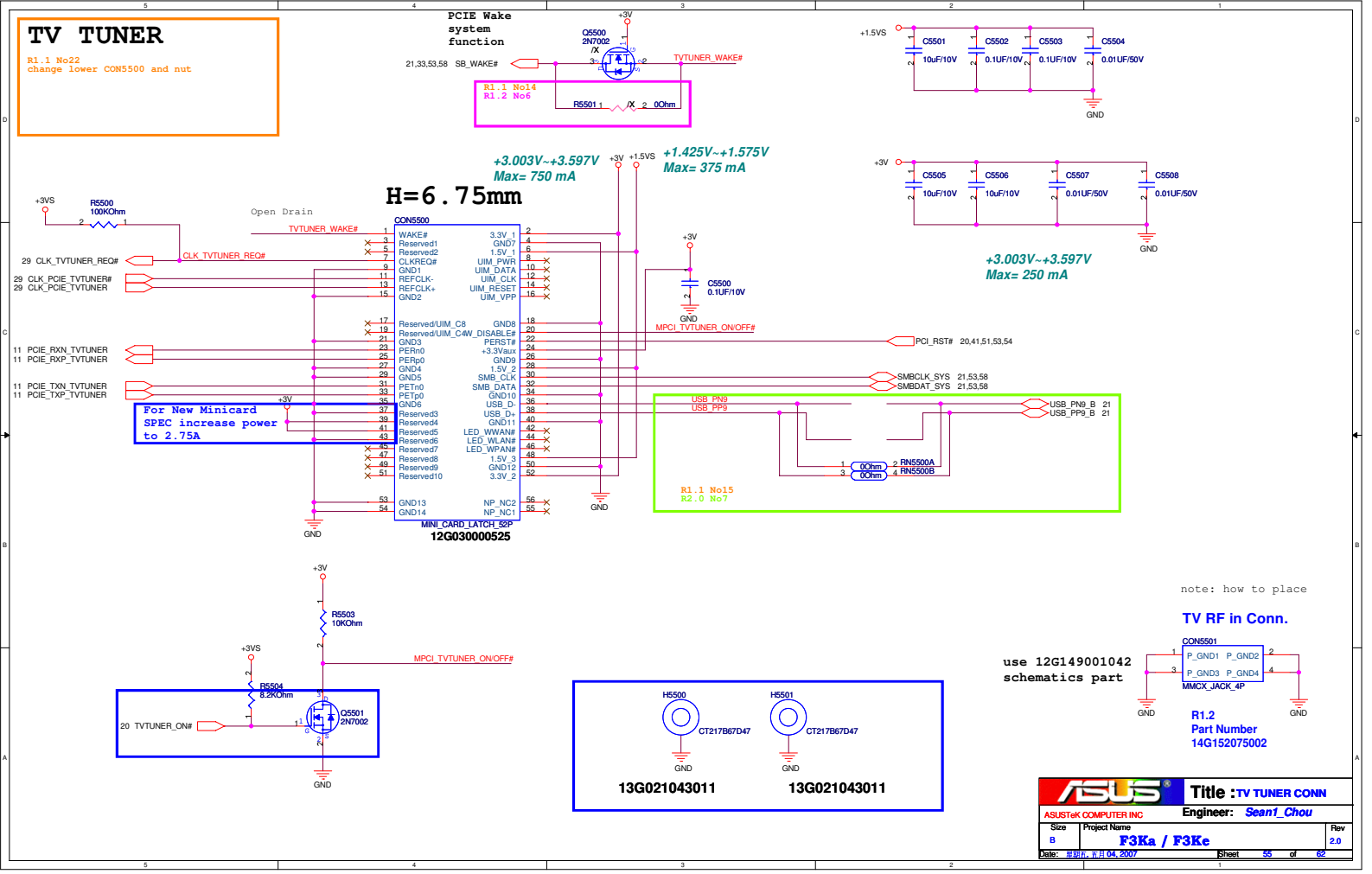
ASUSTeK COMPUTER INC	Title : MINI PCIEX & BT CONN.		
	Engineer: Sean1_Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: Fri, 04, 2007	Sheet 53 of 62		

WWAN--Windigo
Only support in S0 Stage

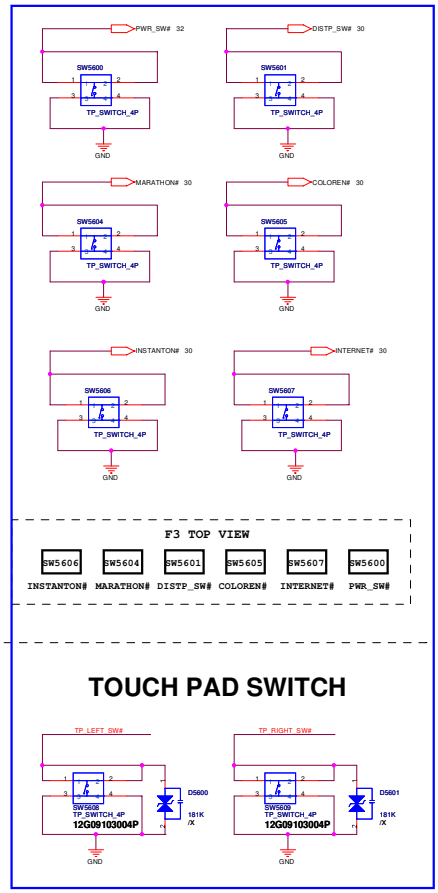


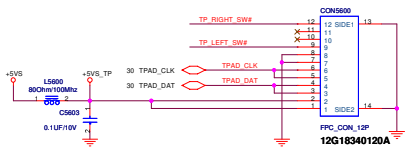
ASUSTek Computer INC.	Title : MINI Card-Windigo	
	Engineer: Sean1_Chou	
Size: B	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期五, 五月 04, 2007	Sheet 54 of 62	

<< Kennedy_Zhang >>

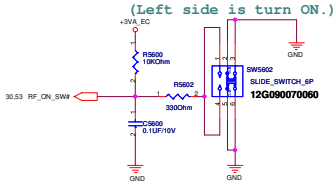


<< Kennedy_Zhang >>

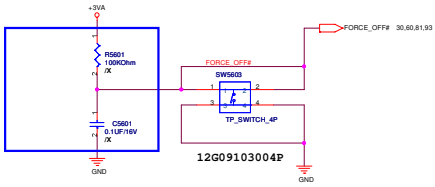




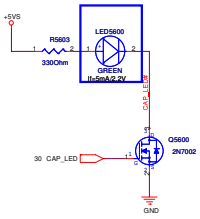
RF ON/OFF SWITCH
For Side SW
(Left side is turn ON.)



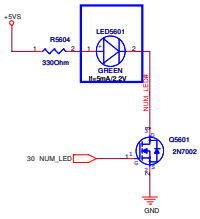
SHUT_DOWN#



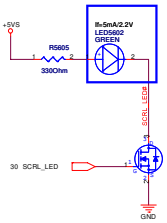
for Cap. Lock



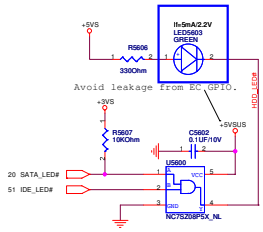
for Num Lock



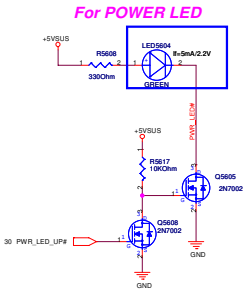
for Scroll Lock



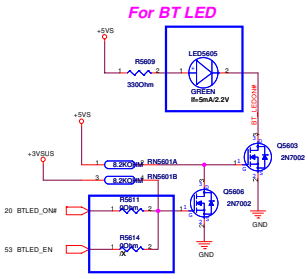
For SATA/IDE LED



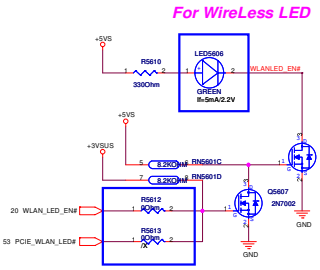
For POWER LED



For BT LED

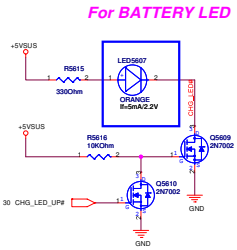


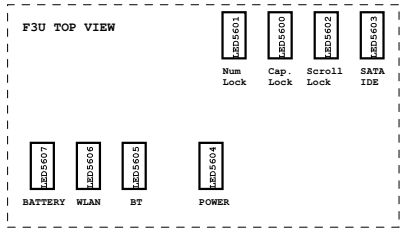
For WireLess LED



Green: 07G015700341
Orange: 07G015700064

For BATTERY LED

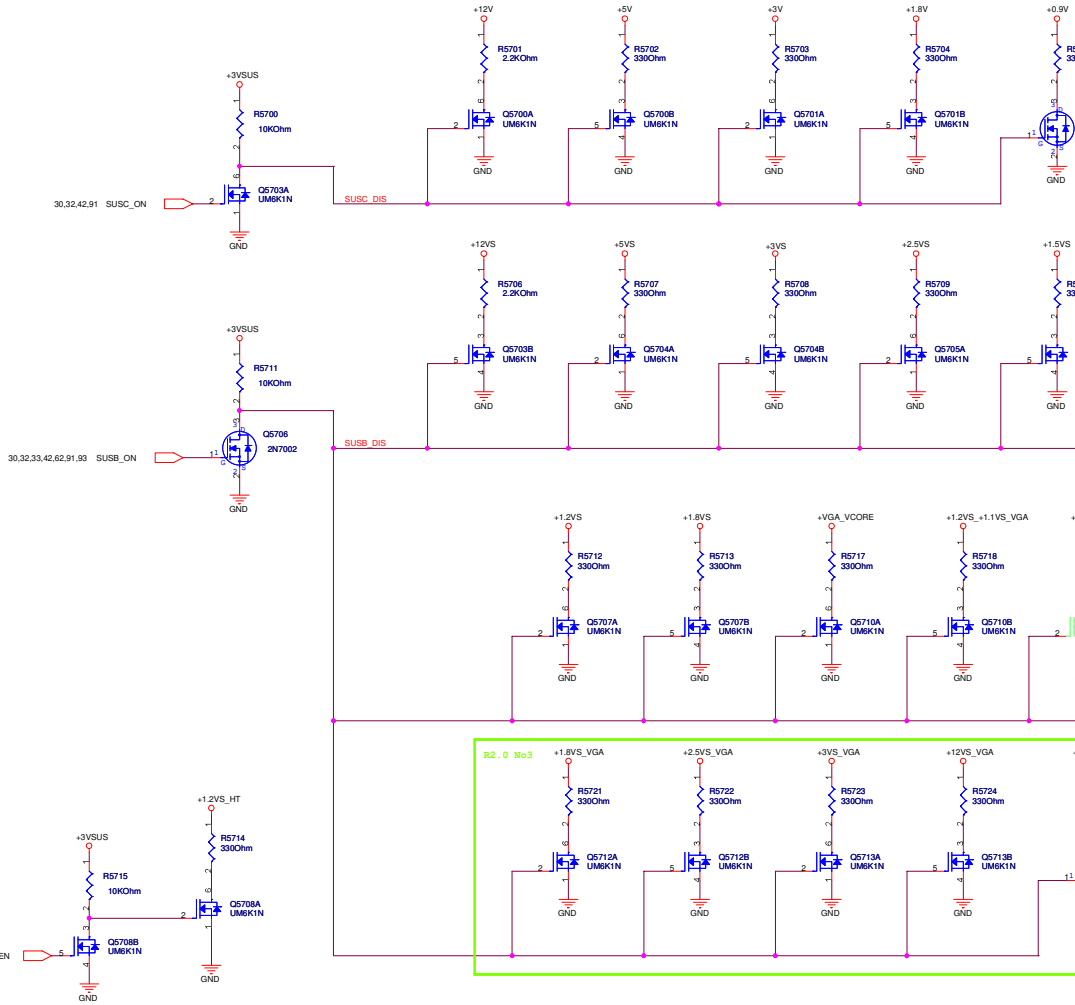




ASUSTeK COMPUTER INC	Title : LED&SW&TOUCHPAD		
	Engineer: Sean1_Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: Thu, 04, 2007	Sheet 58 of 62		

<< Kennedy_Zhang >>

DISCHARGE CIRCUIT



ASUSTeK COMPUTER INC

Title : DISCHARGE CIRCUIT

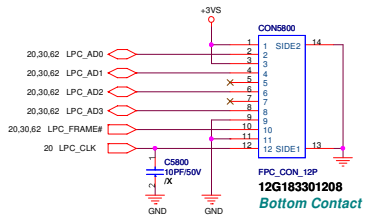
Engineer: Sean1_Chou

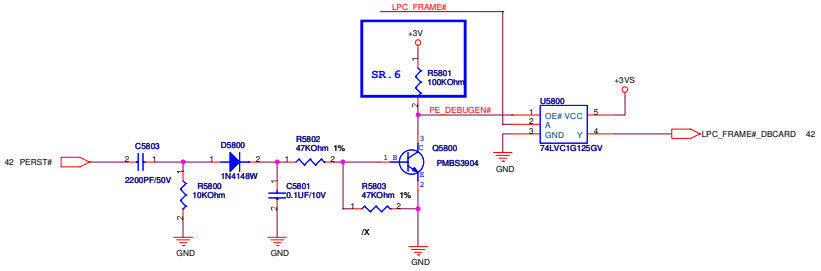
Size	Project Name	Rev
Custom	F3Ka / F3Ke	2.0

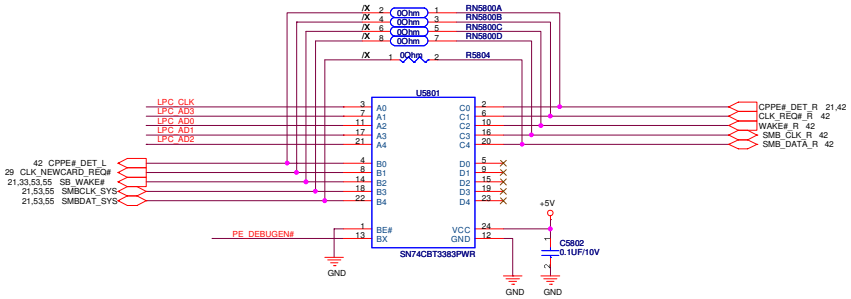
Date: 星期六, 六月 04, 2007 Sheet 57 of 62

<< Kennedy_Zhang >>

LPC DEBUG CONNCTOR







ASUSTeK COMPUTER INC

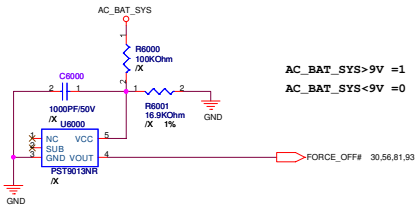
Title : DEBUG CIRCUITS

Engineer: Sean1_Chou

Size	Project Name	Rev
Custom	F3Ka / F3Ke	2.0

Date: 星期六, 六月 04, 2007 Sheet 58 of 62

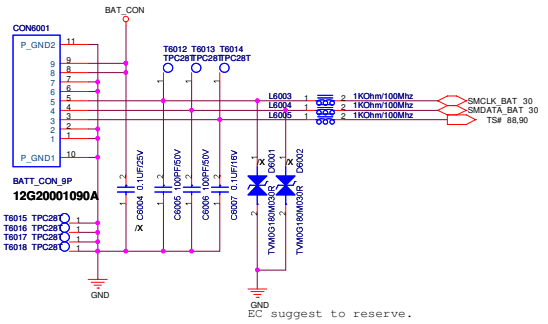
Without Battery & Pull out Adapter



AC_BAT_SYS>9V =1

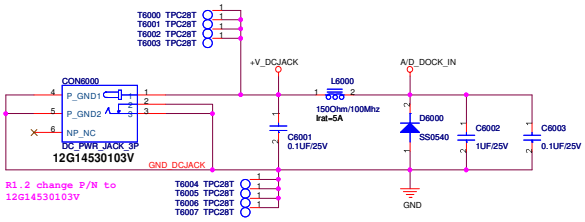
AC_BAT_SYS<9V =0

Battery Connector



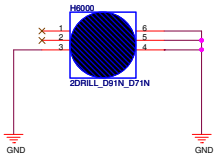
EC suggest to reserve.

DC Power Jack

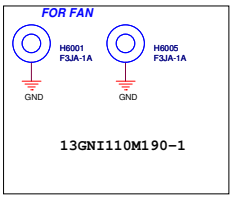


R1.2 change P/N to 12G14530103V

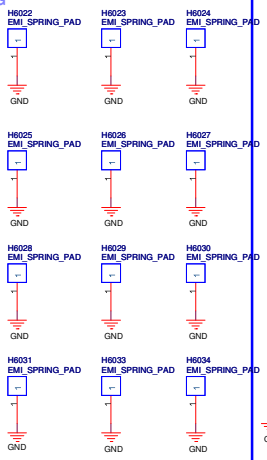
FOR LEFT UNDER



FOR FAN

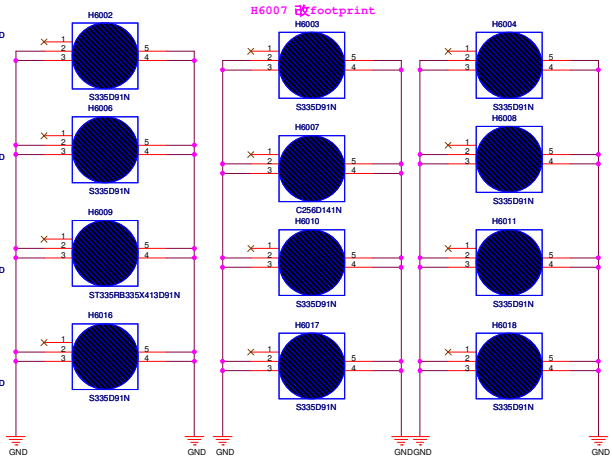


EMI SPRING

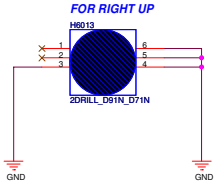


FOR SCREW HOLE

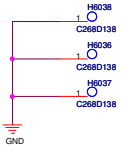
H6007 RK footprint



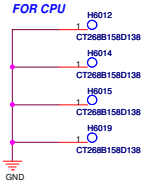
FOR RIGHT UP



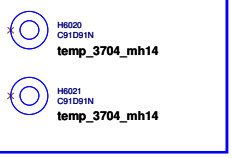
FOR VGA



FOR CPU



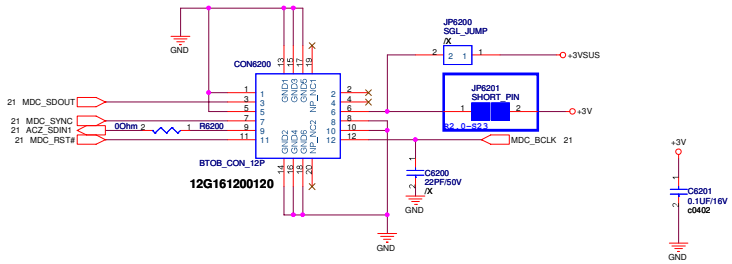
FOR FAN Fix Hole position



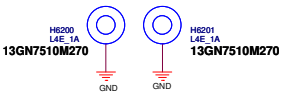
ASUSTeK COMPUTER INC	Title : DC IN & SCREW HOLE		
	Engineer: Sean1_Chou		
Size: Custom	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: 星期六, 六月 04, 2007	Sheet 60 of 62		

<< Kennedy_Zhang >>

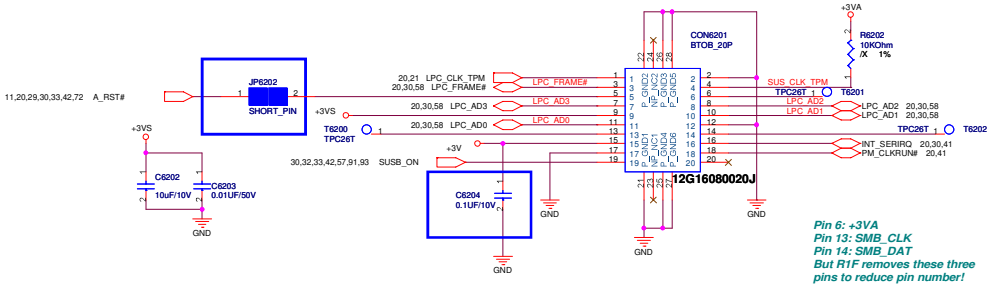
MDC CONN.



For MDC

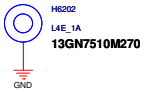


TPM CONN.



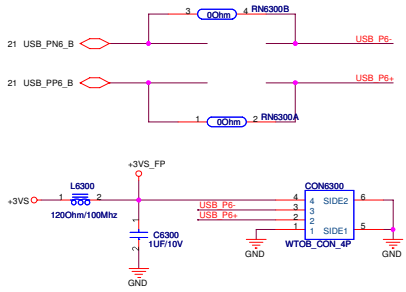
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

For TPM



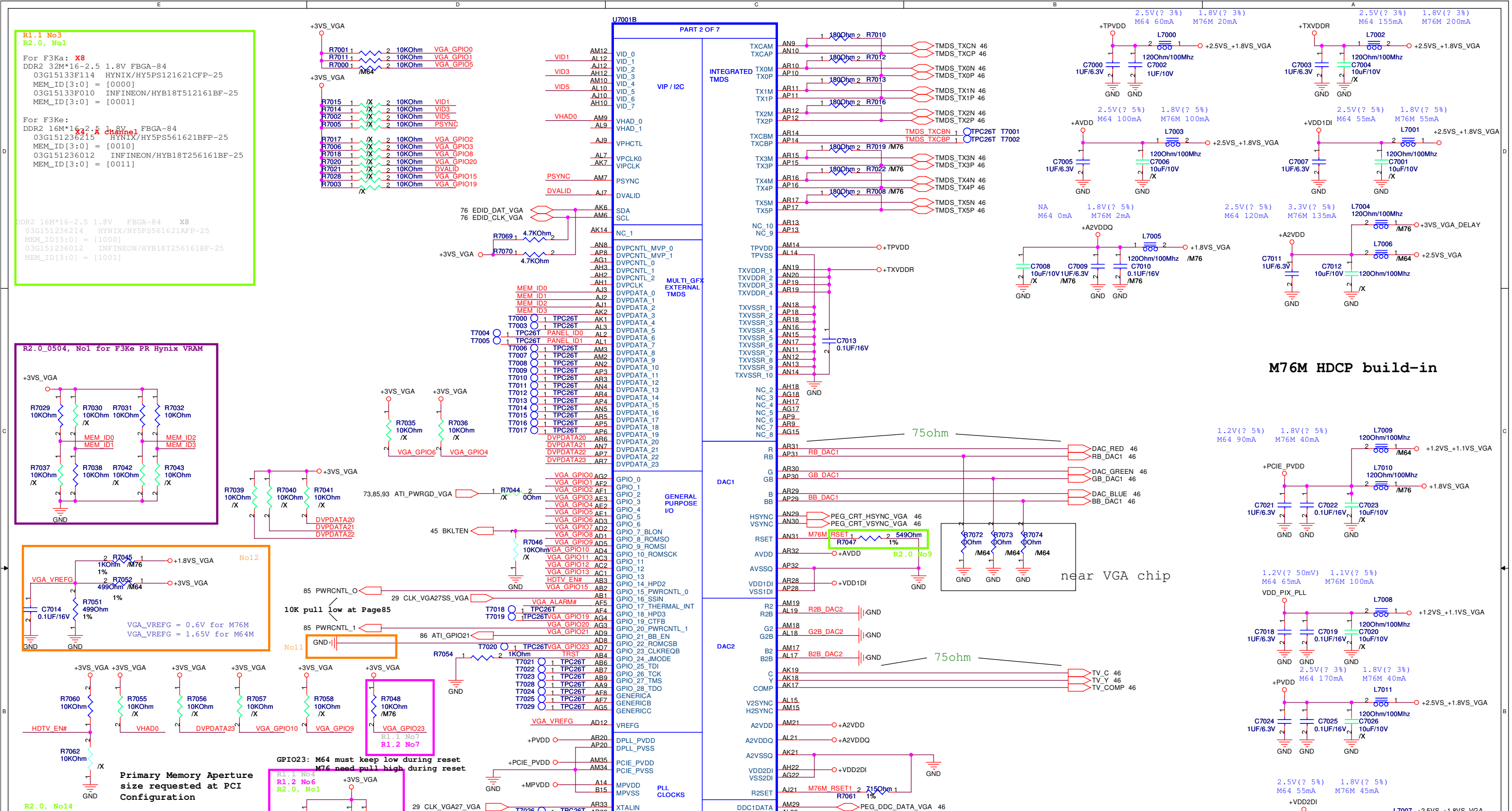
ASUSTeK COMPUTER INC	Title : TPM&MDC CONNECTOR	
	Engineer: Sean1_Chou	
Size: Custom	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期五, 六月 04, 2007	Sheet 62 of 82	

<< Kennedy_Zhang >>



ASUSTek Computer INC.	Title : Finger Printer	
	Engineer: Sean1_Chou	
Size: B	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: 星期五, 六月 04, 2007	Sheet 63 of 62	

<< Kennedy_Zhang >>



R2.0, No14

M64	GPIO_13	GPIO_12	GPIO_11	M76
128MB	* 0	0	0	128MB
256MB	0	1	0	64MB
64MB	1	0	0	* 512MB
reserved	1	1	0	2GB
	0	0	1	256MB
	1	0	1	1GB
	1	1	1	4GB

M76 Strap Pin (All internal default Pull-Down)

VSYNC *0: Driver would not recognize a VIP device on the VIP Host interface
1: Driver would recognize a VIP device on the VIP Host interface

VHAD0 *0: VIP Device Disable
1: VIP Device Enable

PSYNC *0: VGA Enable
1: VGA Disable

GPIO_0 0: 50% Tx Output Swing
*1: Full Tx Output Swing

GPIO_1 0: Tx De-emphasis Disable
*1: Tx De-emphasis Enable

GPIO_22 ROMCSB *0: Disable external BIOS ROM device
1: Enable external BIOS ROM device

GPIO_13 GPIO_12 GPIO_11 *If GPIO_22 = 0, then Config[2:0] defines the primary memory aperture size. (GPIO_9_ROMSI = don't care).
If GPIO_22 = 1, then Config[3:0] defines the ROM type.

VID_1 *0: MSI Disable
1: MSI Enable

VID_3 *0: Disable HD Audio
1: Enable HD Audio

VID_5 *0: Enable 32-bit BARs
1: Enable 64-bit BARs

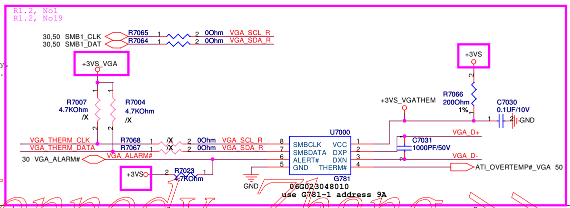
DVALID *0: Disable CLKREQ# power management capability.
1: Enable CLKREQ# power management capability.

GPIO_5 0: For M76M
*1: For M64M/M66M

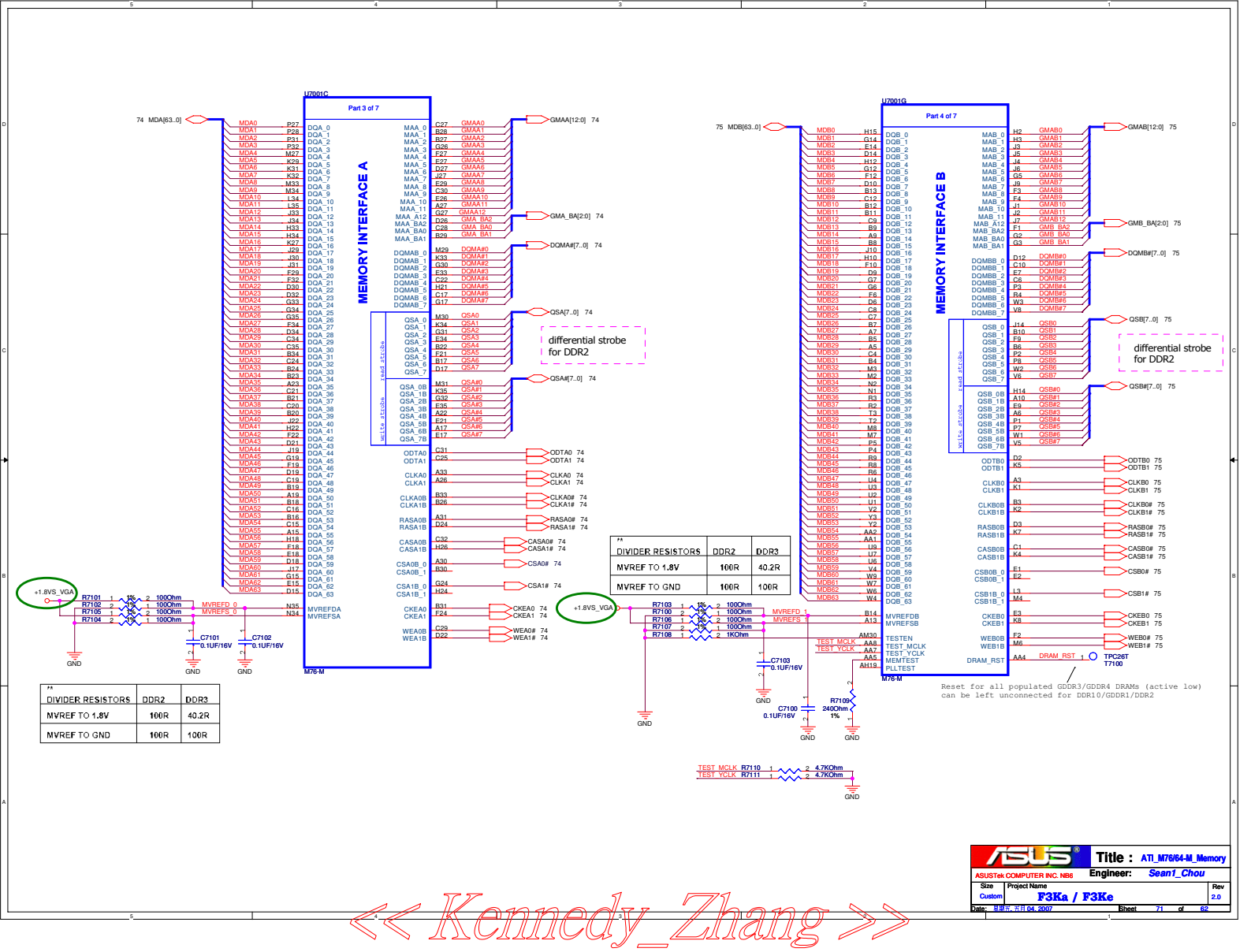
GPIO_4 *0: Debug-Access Disable
1: Debug-Access Enable

{VID_0, VID_2, VID_4, VID_6, VID_7, HSYNC, GPIO_2, GPIO_6, GPIO_8_ROMSO, H2SYNC, V2SYNC} can reserve Pull-Up, but MUST keep Low during Reset

{GPIO_28_TDO, GPIO_21_BB_EN, GENERICC, V2SYNC, H2SYNC} MUST keep Low during Reset & can NOT reserve Pull-Up



Title :	ATI_M76/64-M_MAIN
ASUSTek COMPUTER INC	Engineer: Sean1_Chou
Size: C	Project Name: F3Ka / F3Ke — Rev 2.0
Date: 星期五, 五月 04, 2007	Sheet 70 of 62



ASUSTeK COMPUTER INC. NB6

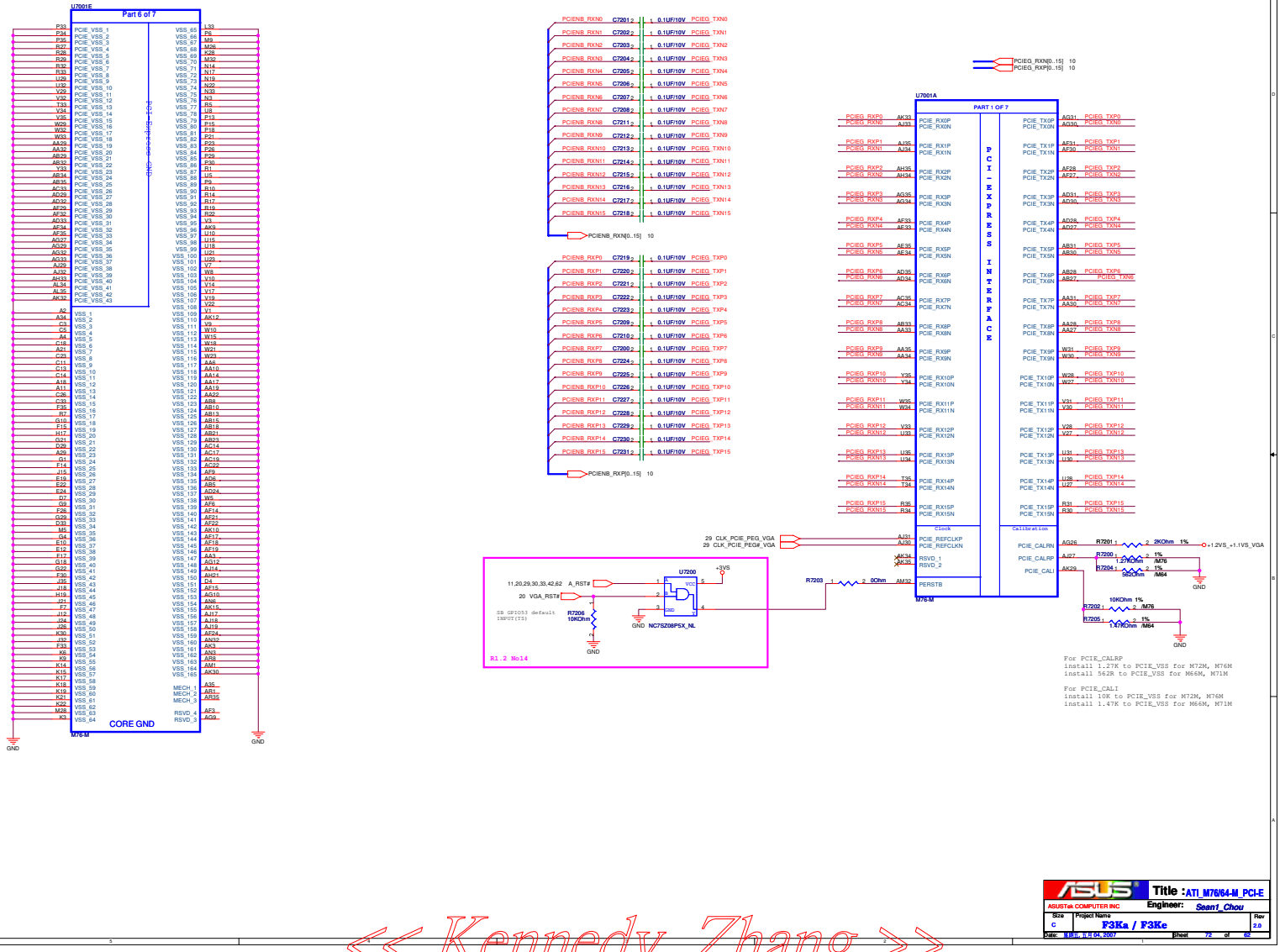
Title : ATI_M76/64-M_Memory

Engineer: Sean1_Chou

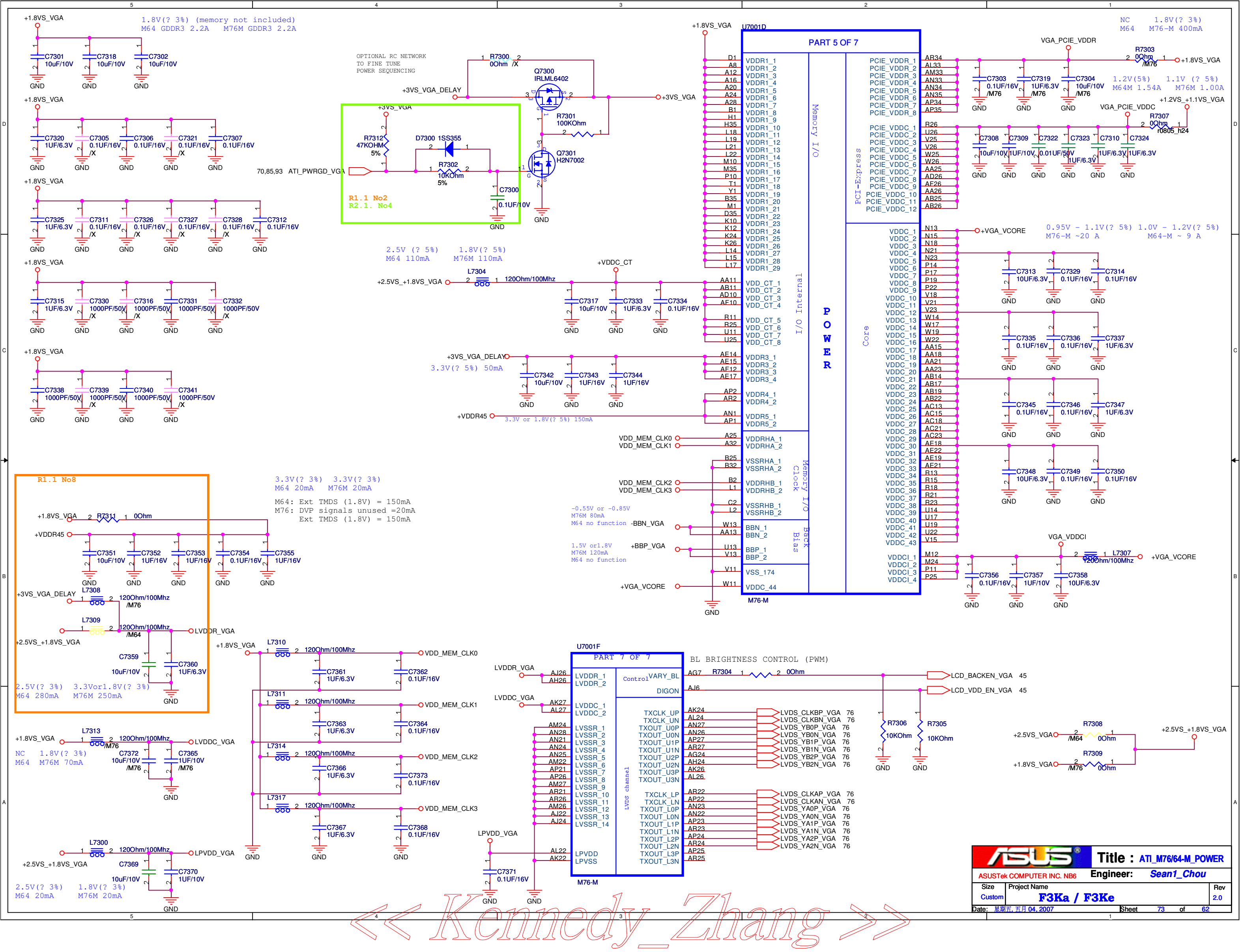
Size	Project Name	Rev
Custom	F3Ka / F3Ke	2.0

Date: 星期六, 六月 04, 2007 Sheet 71 of 82

<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC	Title : ATI_M76/64-M_PCI-E		
	Engineer: Sean1_Chou		
Size: C	Project Name: F3Ka / F3Ke		Rev: 2.0
Date: Wed, Jul 04, 2007	Sheet 72 of 82		



1.8V(? 3%) (memory not included)
M64 GDDR3 2.2A M76M GDDR3 2.2A
OPTIONAL RC NETWORK
TO FINE TUNE
POWER SEQUENCING
R1.1 No2
R2.1. No4
70,85,93 ATI_PWRGD_VGA
U7001D
PART 5 OF 7
Memory I/O
PCI-Express
Internal I/O
POWER
Core
Memory Clock I/O
Back Bias
M76-M
NC 1.8V(? 3%)
M64 M76-M 400mA
VGA_PCIE_VDDR
1.2V(5%) 1.1V (? 5%)
M64M 1.54A M76M 1.00A
+1.2VS_+1.1VS_VGA
VGA_PCIE_VDDC
+VGA_VCORE
0.95V ~ 1.1V(? 5%) 1.0V ~ 1.2V(? 5%)
M76-M ~20 A M64-M ~ 9 A
2.5V (? 5%) 1.8V(? 5%)
M64 110mA M76M 110mA
+VDDC_CT
+2.5VS_+1.8VS_VGA
+3VS_VGA_DELAY
3.3V(? 5%) 50mA
+VDDR45
3.3V or 1.8V(? 5%) 150mA
VDD_MEM_CLK0
VDD_MEM_CLK1
VDD_MEM_CLK2
VDD_MEM_CLK3
-0.55V or -0.85V
M76M 80mA
M64 no function
-BBN_VGA
1.5V or1.8V
M76M 120mA
M64 no function
+BBP_VGA
VGA_VDDCI
R1.1 No8
3.3V(? 3%) 3.3V(? 3%)
M64 20mA M76M 20mA
M64: Ext TMDS (1.8V) = 150mA
M76: DVP signals unused =20mA
Ext TMDS (1.8V) = 150mA
2.5V(? 3%) 3.3Vor1.8V(? 3%)
M64 280mA M76M 250mA
NC 1.8V(? 3%)
M64 M76M 70mA
2.5V(? 3%) 1.8V(? 3%)
M64 20mA M76M 20mA
LVDDR_VGA
LVDDC_VGA
LPVDD_VGA
U7001F
PART 7 OF 7
LVDS channel
BL BRIGHTNESS CONTROL (PWM)
LCD_BACKEN_VGA 45
LCD_VDD_EN_VGA 45
LVDS_CLKBP_VGA 76
LVDS_CLKBN_VGA 76
LVDS_YB0P_VGA 76
LVDS_YB0N_VGA 76
LVDS_YB1P_VGA 76
LVDS_YB1N_VGA 76
LVDS_YB2P_VGA 76
LVDS_YB2N_VGA 76
LVDS_CLKAP_VGA 76
LVDS_CLKAN_VGA 76
LVDS_YA0P_VGA 76
LVDS_YA0N_VGA 76
LVDS_YA1P_VGA 76
LVDS_YA1N_VGA 76
LVDS_YA2P_VGA 76
LVDS_YA2N_VGA 76
ASUSTeK COMPUTER INC. NB6
Title : ATI_M76/64-M_POWER
Engineer: Sean1_Chou
Size Custom
Project Name F3Ka / F3Ke
Rev 2.0
Date: 星期五, 五月 04, 2007
Sheet 73 of 62
<< Kennedy_Zhang >>

DDR2 32M*16-2.5 1.8V PGTFBGA84
03G15133F010 INFINEON/HYB18T512161BF-25

FBGA-84
03G15133F114 HYNIX/HY5PS121621CFP-25

DDR2 16M*16-2.5 1.8V FBGA-84
03G151236012 INFINEON/HYB18T256161BF-25
03G151236214 HYNIX/HY5PS561621AFP-25

A0

03G15133F110

Swapable A1

U7400 / U7401 / U7402 / U7403 — HY5PS121621BFP-25L

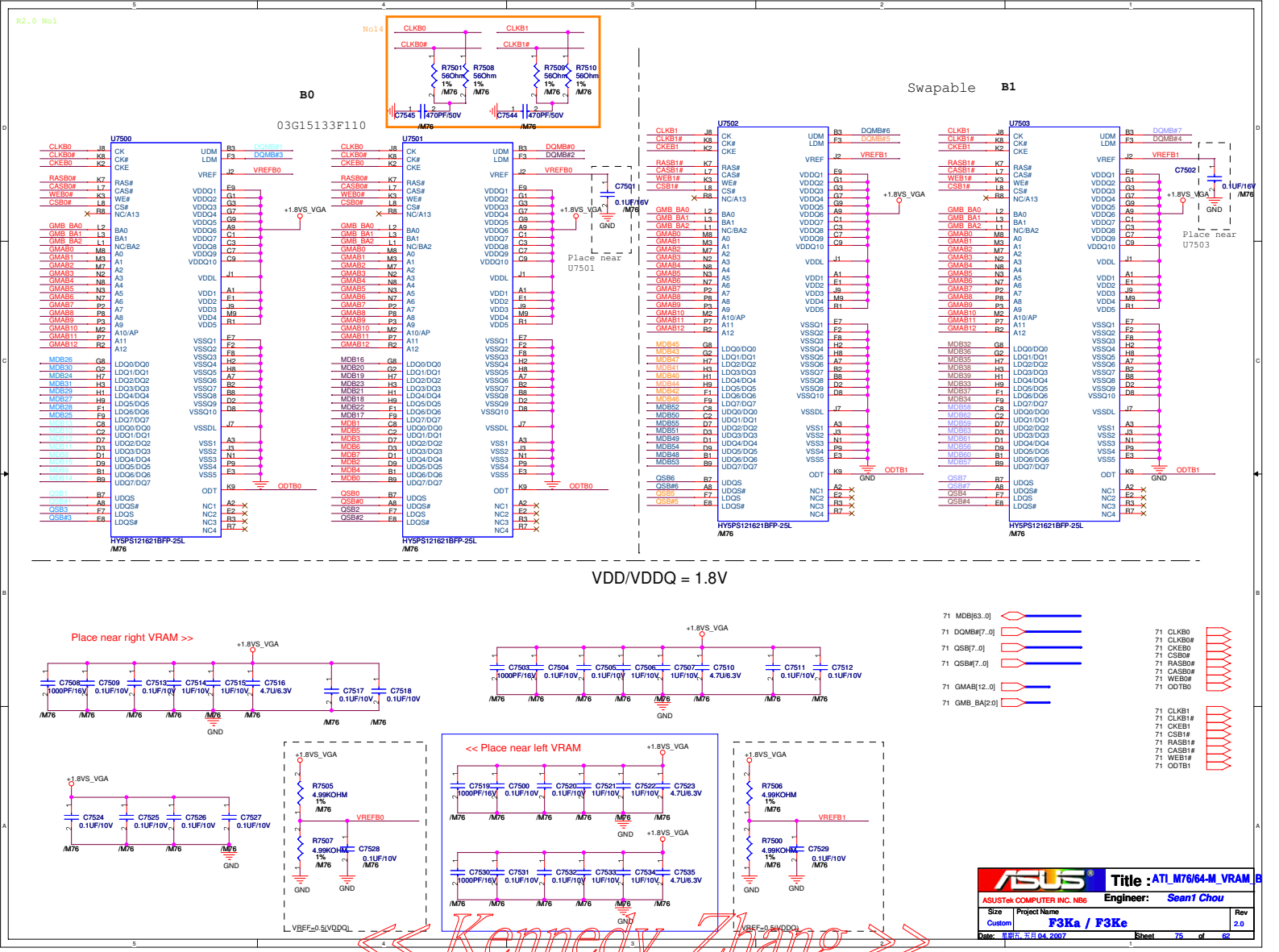
VDD/VDDQ = 1.8V

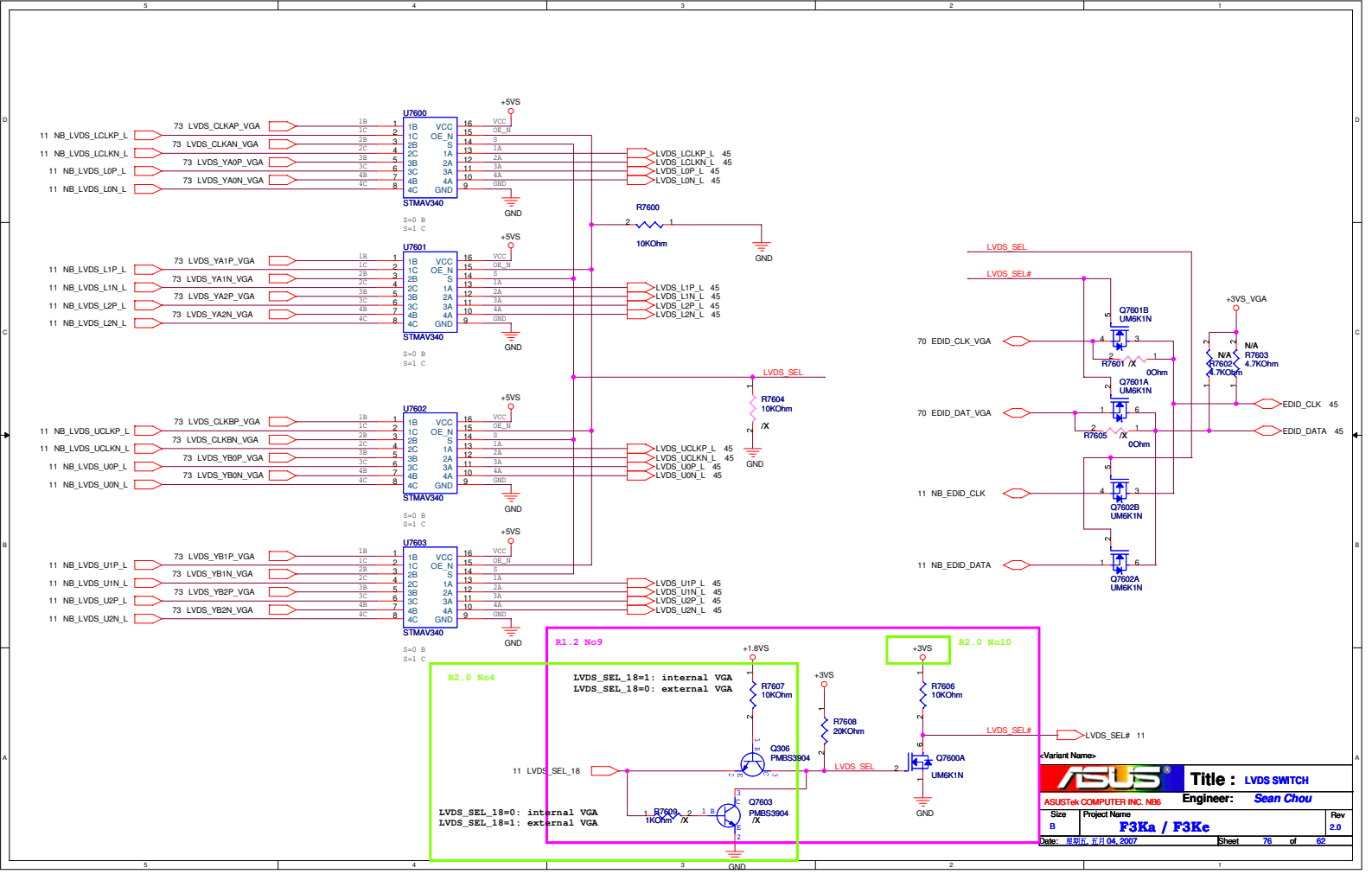
Place near right VRAM >>

<< Place near left VRAM

<< Kennedy_Zhang >>

Title :	ATI_M76/64-M_VRAM_A
ASUSTek COMPUTER INC. NB6	Engineer: Sean1_Chou
Size: Custom	Project Name: F3Ka / F3Ke
Rev: 2.0	
Date: 星期六, 五月 04, 2007	Sheet 74 of 82

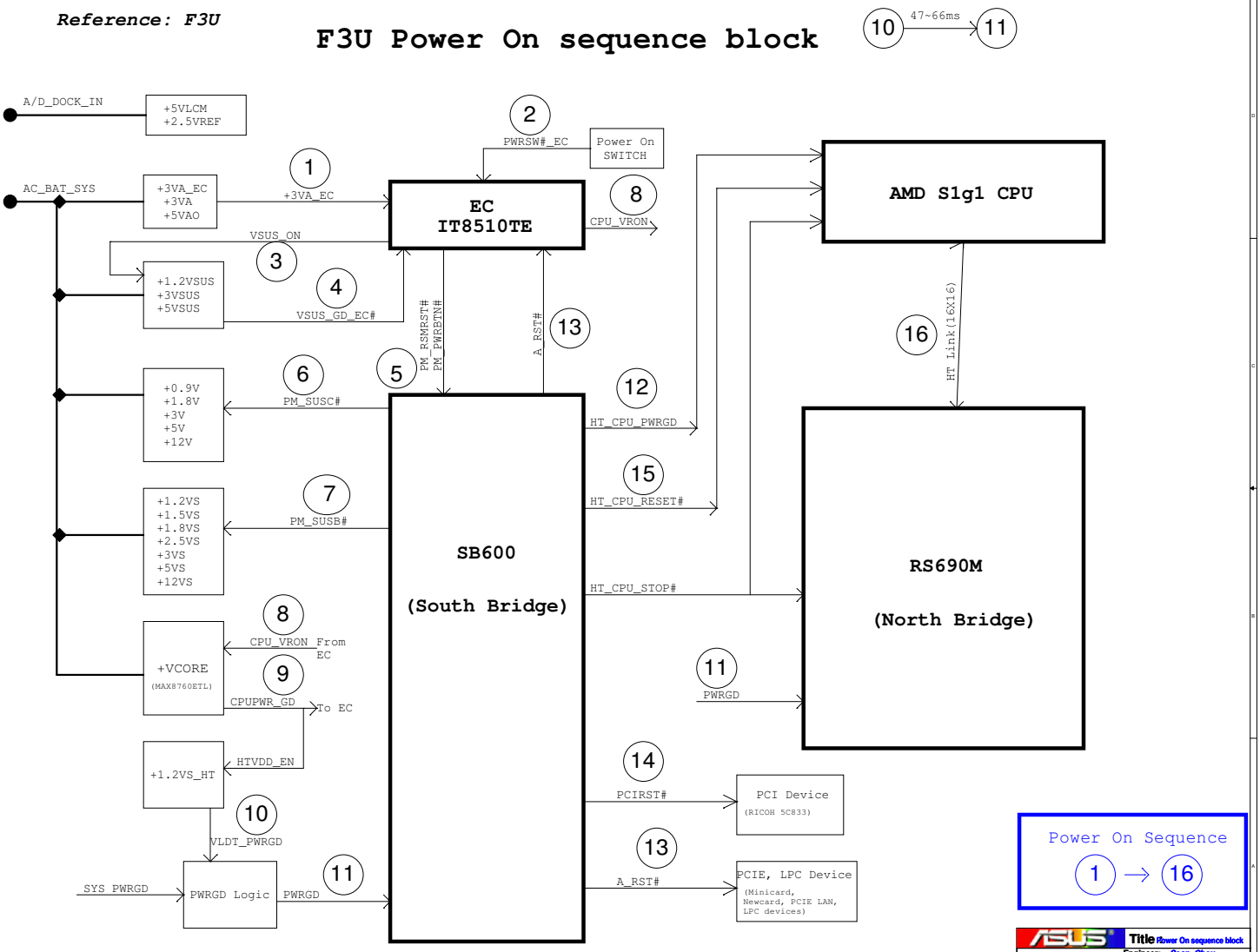




<< Kennedy_Zhang >>

Reference: F3U

F3U Power On sequence block



ASUSTeK COMPUTER INC.

Title: Power On sequence block

Engineer: Sean_Chou

Size	Project Name	Rev
C	F3Ka / F3Ke	2.0

Date: Wed, Jul 04, 2007 Sheet 78 of 82

<< Kennedy_Zhang >>

REVISION LIST

F3U revision list

R1.0 2006/09/13

R1.1 2006/10/02

NO1 Page3 : R321 change to pull up to +3VSUS

NO2 Page20 : Mount R2009 for SATA 25MHz cystal oscilation with 10Mohm

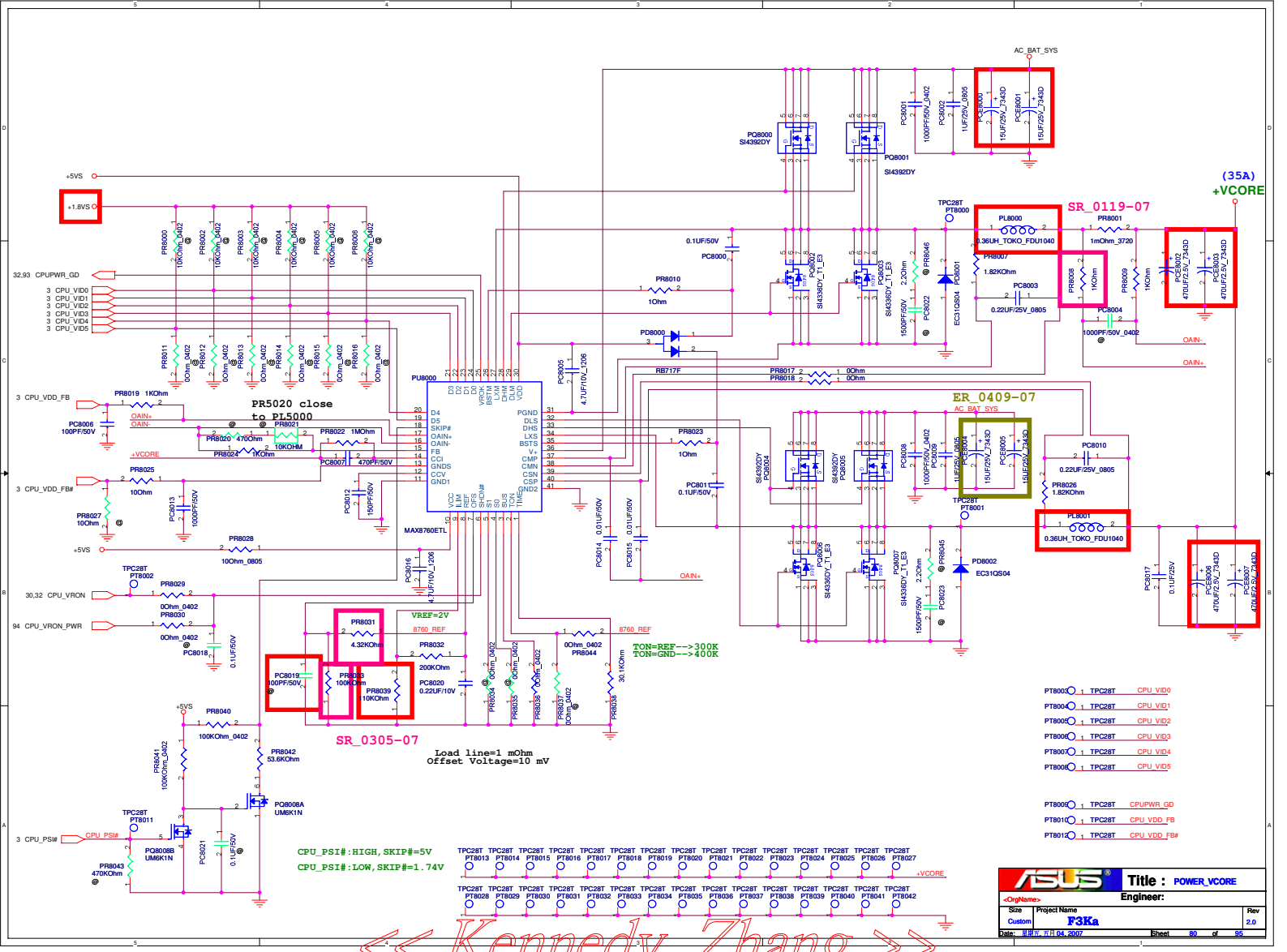
NO3 Page21: Exchange EXTSMI# and KB_SCI# GEVENT at SB600 for Power leakage problem
Page30: Add 10Kohm resistor pull up on EXTSMI# to follow EC pin assignment v1.13

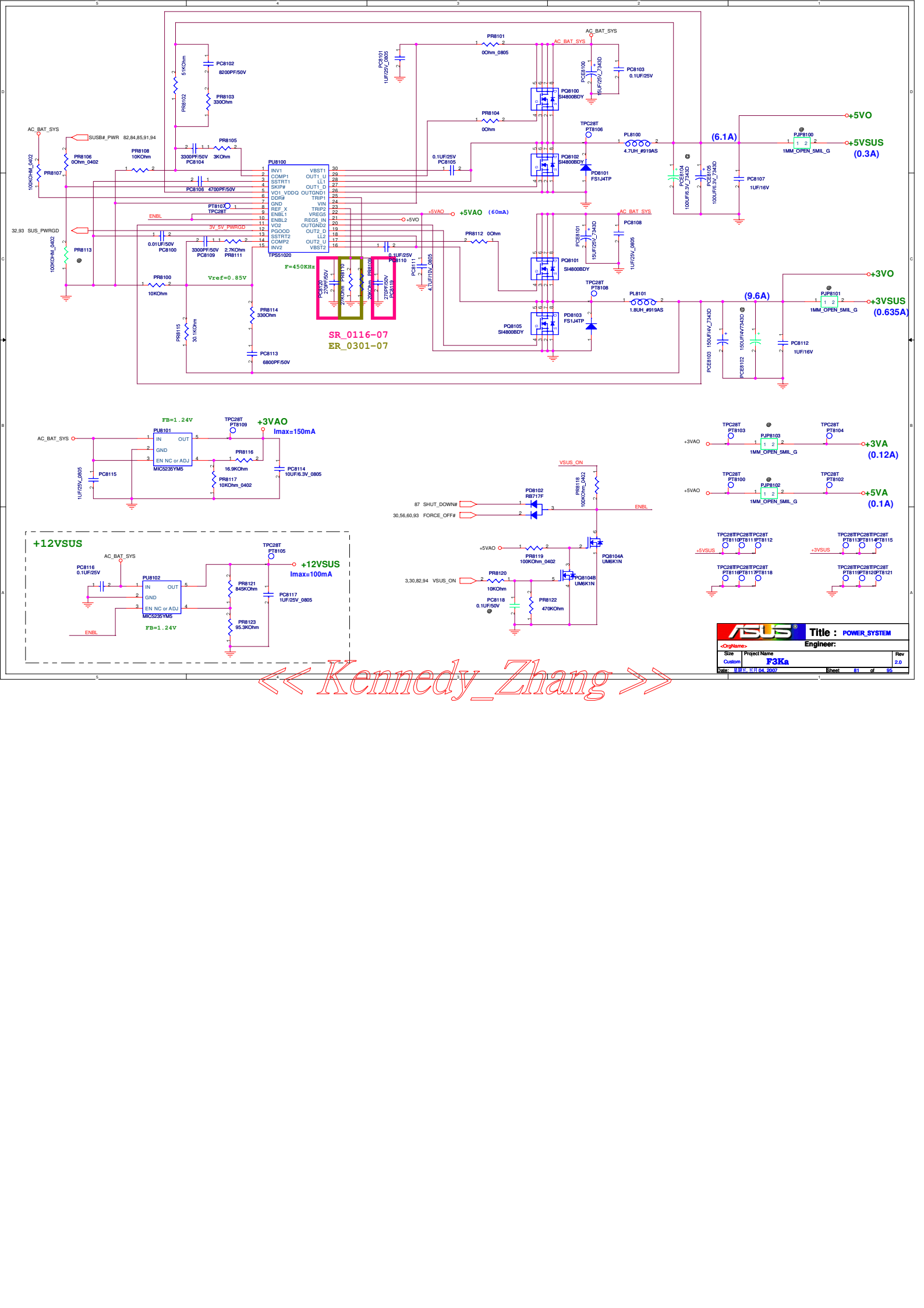
NO4 Page20,21: Change BTLED_ON# and WLAN_LED_EN# to GPIO31, GPIO32

NO5 Page30: Cut off Force_off# path to EC_RST# logic

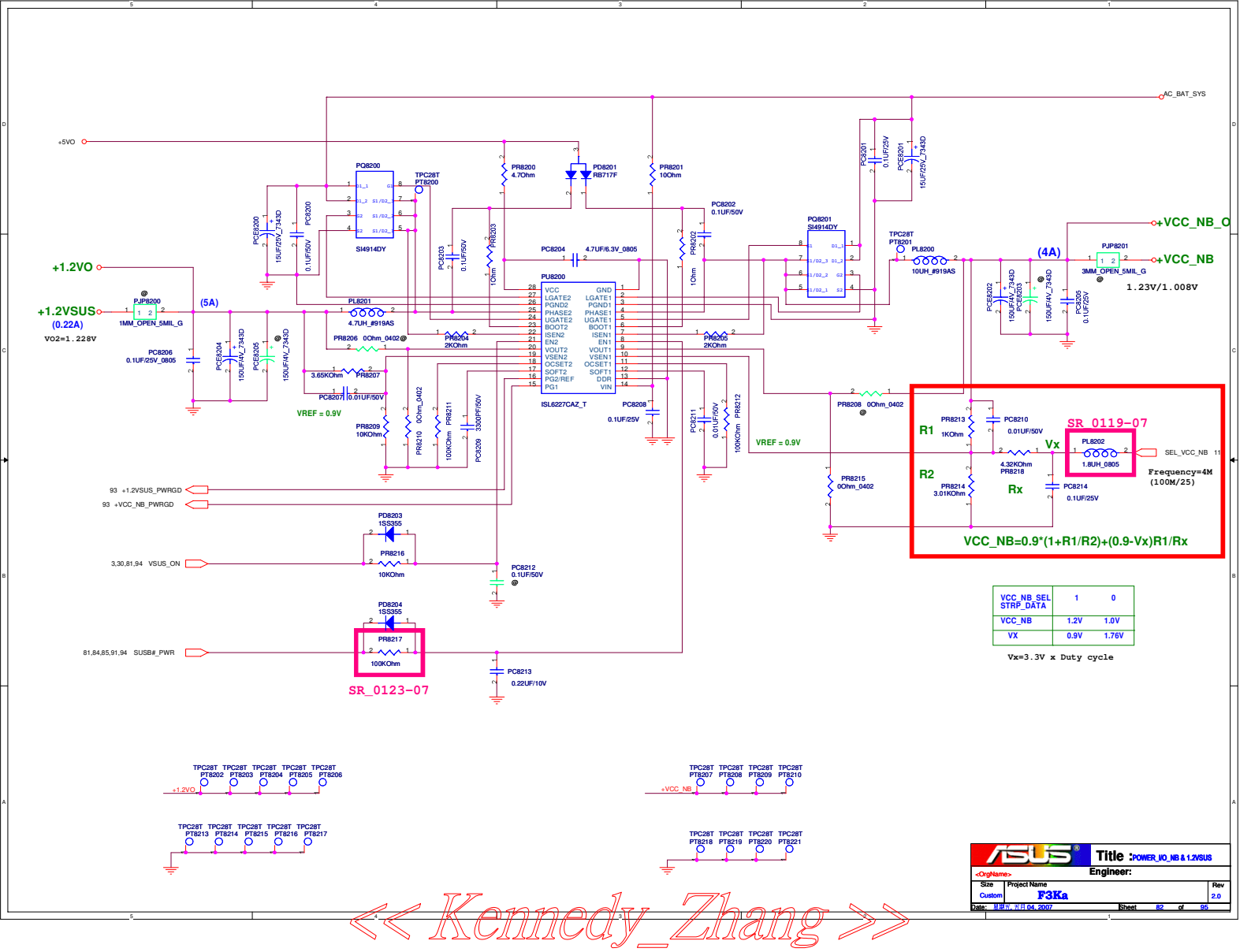
NO6 Page42: Add R4205 serial resistor at PERST#, SHDN# control pin change to SUSC_ON, AUXIN power change to +3V
Page58: R5801 pull up change to +3V power

ASUSTeK COMPUTER INC.	Title: Power On sequence block	
	Engineer: Sean_Chou	
Size: C	Project Name: F3Ka / F3Ke	Rev: 2.0
Date: Wed, Jul 04, 2007	Sheet 79 of 82	

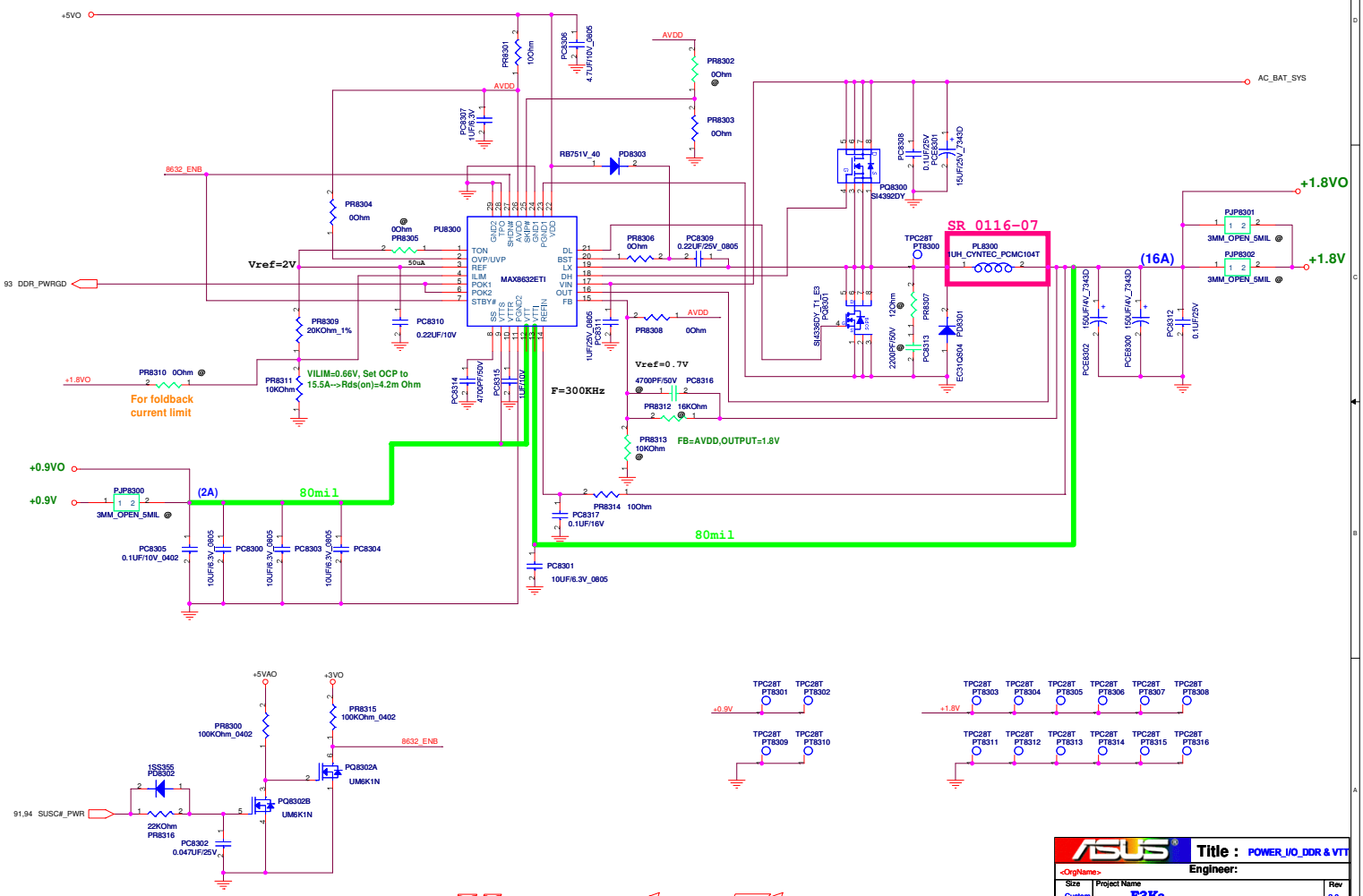

AC_BAT_SYS
(35A)
+VCORE
SR_0119-07
ER_0409-07
SR_0305-07
PR5020 close to PL5000
MAX8760ETL
PU8000
PQ8000 SI4392DY
PQ8001 SI4392DY
PL8000 0.36UH_TOKO_FDU1040
PL8001 0.36UH_TOKO_FDU1040
PD8000 EC31QS04
PD8002 EC31QS04
PQ8008A UM6K1N
PQ8008B UM6K1N
+5VS
+1.8VS
+VCORE
VREF=2V
8760_REF
TON=REF-->300K
TON=GND-->400K
Load line=1 mOhm
Offset Voltage=10 mV
CPU_PSI#:HIGH,SKIP#=5V
CPU_PSI#:LOW,SKIP#=1.74V
Title : POWER_VCORE
Engineer:
Project Name F3Ka
Rev 2.0
Sheet 80 of 95
<< Kennedy_Zhang >>



Title : POWER_SYSTEM		
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Ka	Rev: 2.0
Date: 星期五, 六月 04, 2007	Sheet 81 of 95	

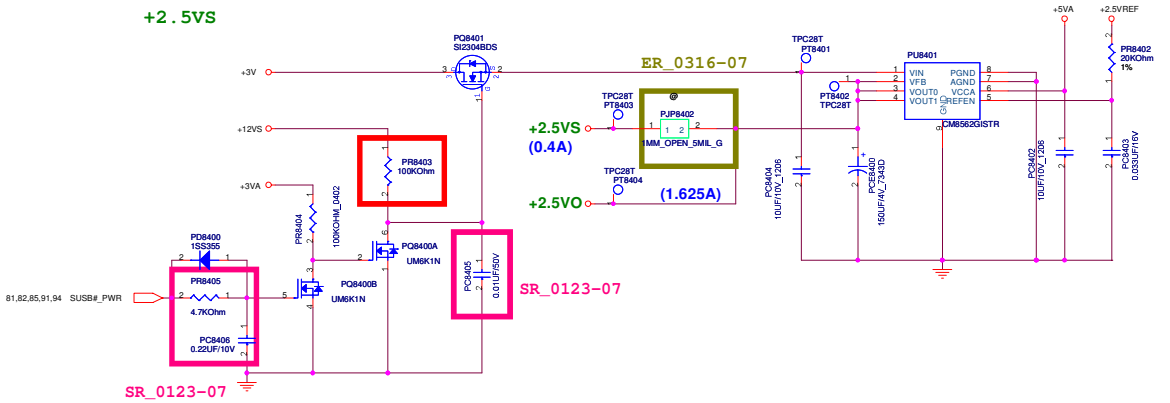


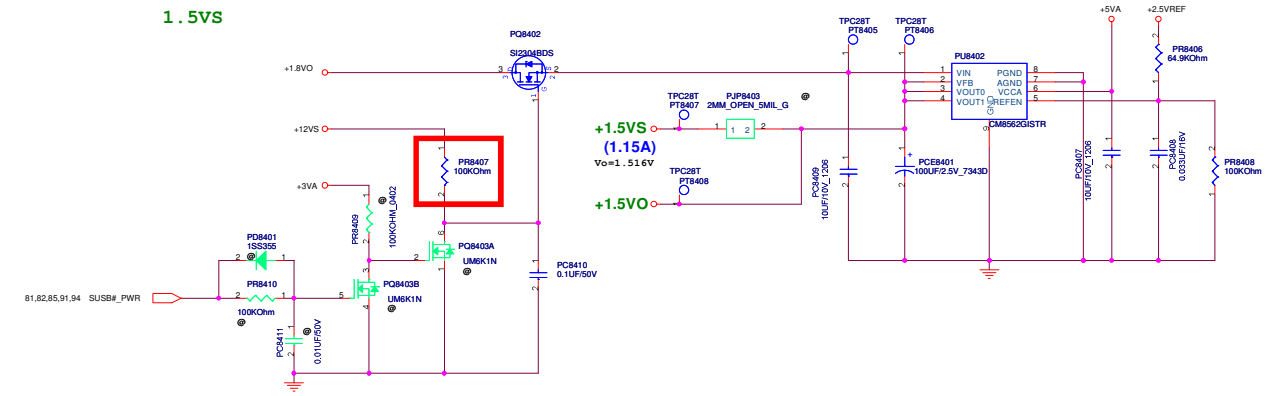
<< Kennedy_Zhang >>



Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Ka	Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 83 of 95	

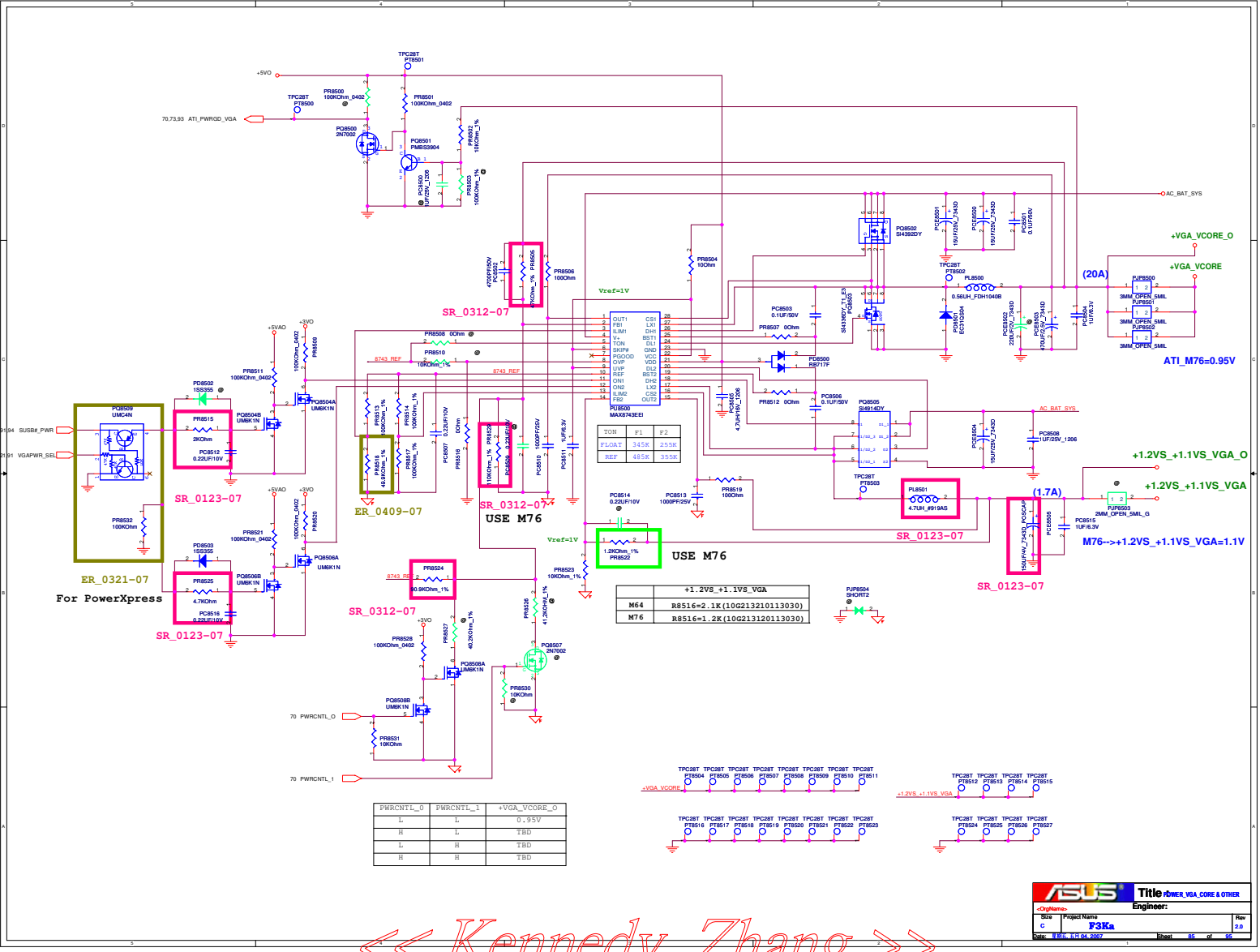
<< Kennedy_Zhang >>





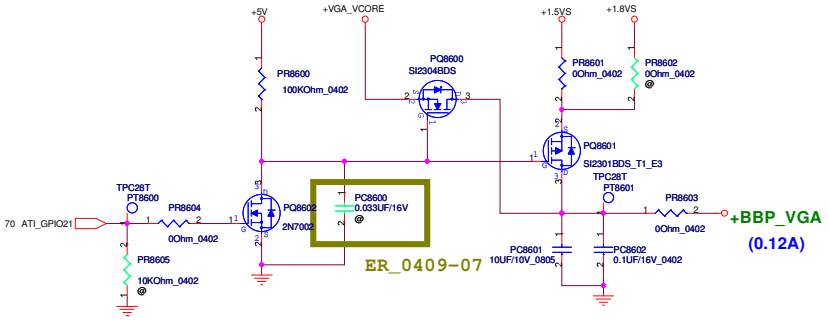
<< Kennedy_Zhang >>

ASUS	Title :	POWER_+2.5VS&+1.5VS
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Ka	Rev: 2.0
Date: 星期六, 五月 04, 2007	Sheet 84 of 95	

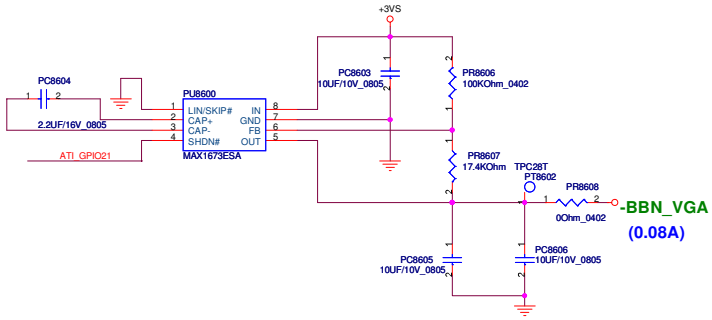


Title: POWER_VGA_CORE & OTHER		
<OrgName>	Engineer:	
Size: C	Project Name: F3Ka	Rev: 2.0
Date: 星期二, 8 月 04, 2007	Sheet 85 of 95	

ATI_GPIO21	+BBP
0	0.95V
1	1.5V



ATI_GPIO21	-BBN
0	GND
1	-0.5V



ASUS

Title : POWER_VGA_OTHER

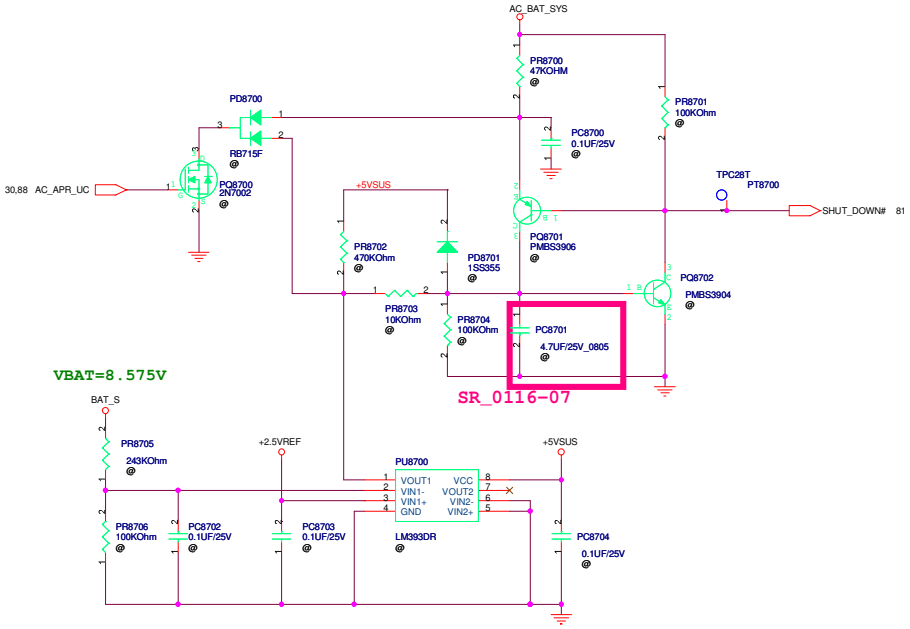
<OrgName>

Engineer:

Size	Project Name	Rev
B	F3Ka	2.0

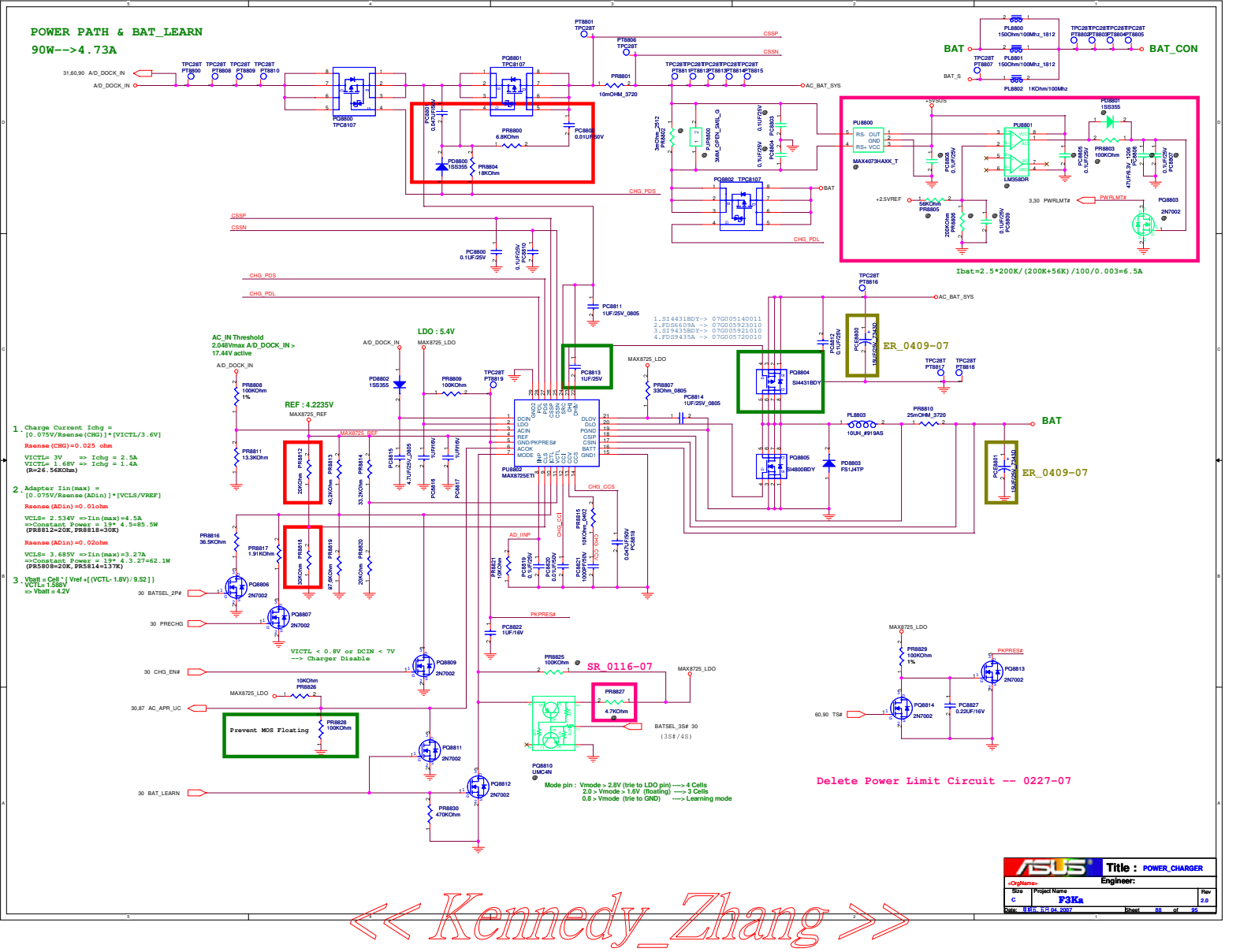
Date: 星期五, 五月 04, 2007 Sheet 86 of 95

BATTERY UVP CIRCUIT



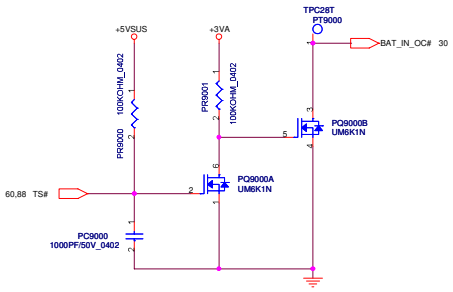
Title : POWER_SHUTDOWN#		
<OrgName>	Engineer:	
Size: B	Project Name: F3Ka	Rev: 2.0
Date: 星期五, 五月 04, 2007	Sheet 87 of 95	

<< Kennedy_Zhang >>

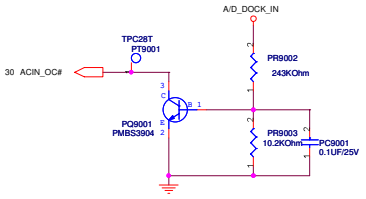

POWER PATH & BAT_LEARN
90W-->4.73A
BAT
BAT_CON
AC_BAT_SYS
CSSP
CSSN
CHG_PDS
CHG_PDL
LDO : 5.4V
REF : 4.2235V
ER_0409-07
SR_0116-07
Ibat=2.5*200K/(200K+56K)/100/0.003=6.5A
Prevent MOS Floating
Delete Power Limit Circuit -- 0227-07
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL < 0.8V or DCIN < 7V
--> Charger Disable
Title : POWER_CHARGER
Engineer:
F3Ka
<< Kennedy_Zhang >>

Title : POWER_PIC				
<OrgName>	Engineer:			
Size	Project Name			Rev
A	F3Ka			2.0
Date: 星期五, 五月 04, 2007		Sheet 89 of 95		

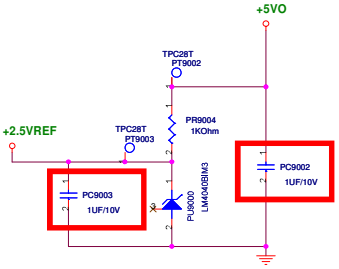
BATTERY IN DETECT



ADAPTER IN DETECT



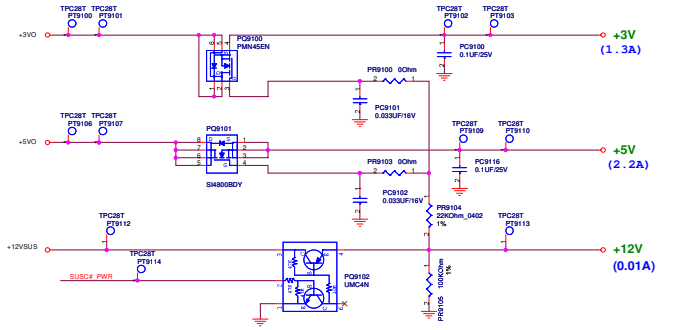
+2.5VREF



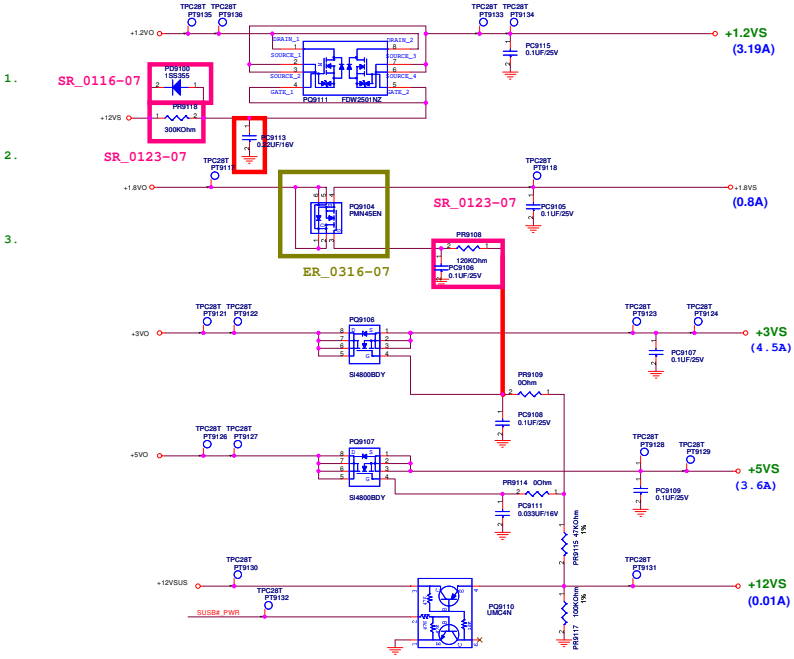
ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Ka	Rev: 2.0
Date: 星期六, 六月 04, 2007	Sheet 90 of 95	

<< Kennedy_Zhang >>

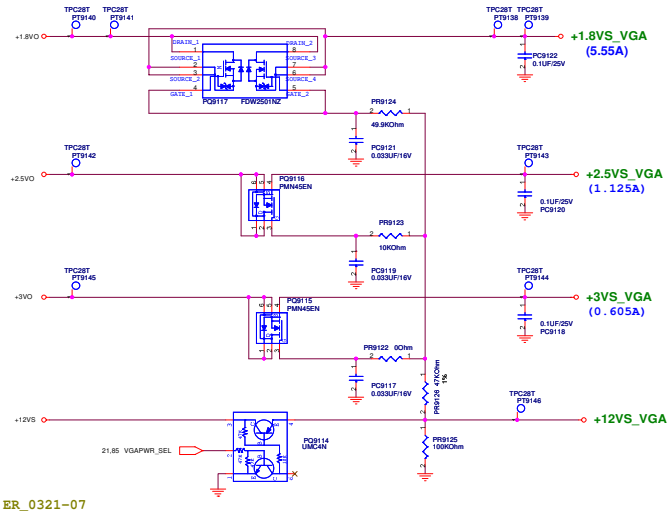
SUSC#_PWR POWER



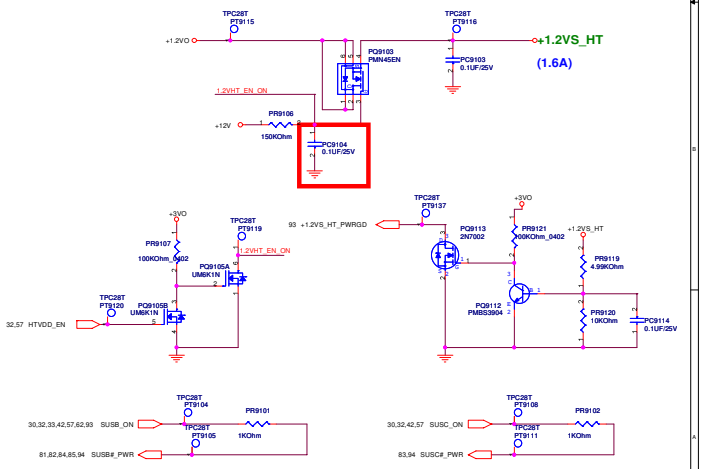
SUSB#_PWR POWER



For PowerXpress

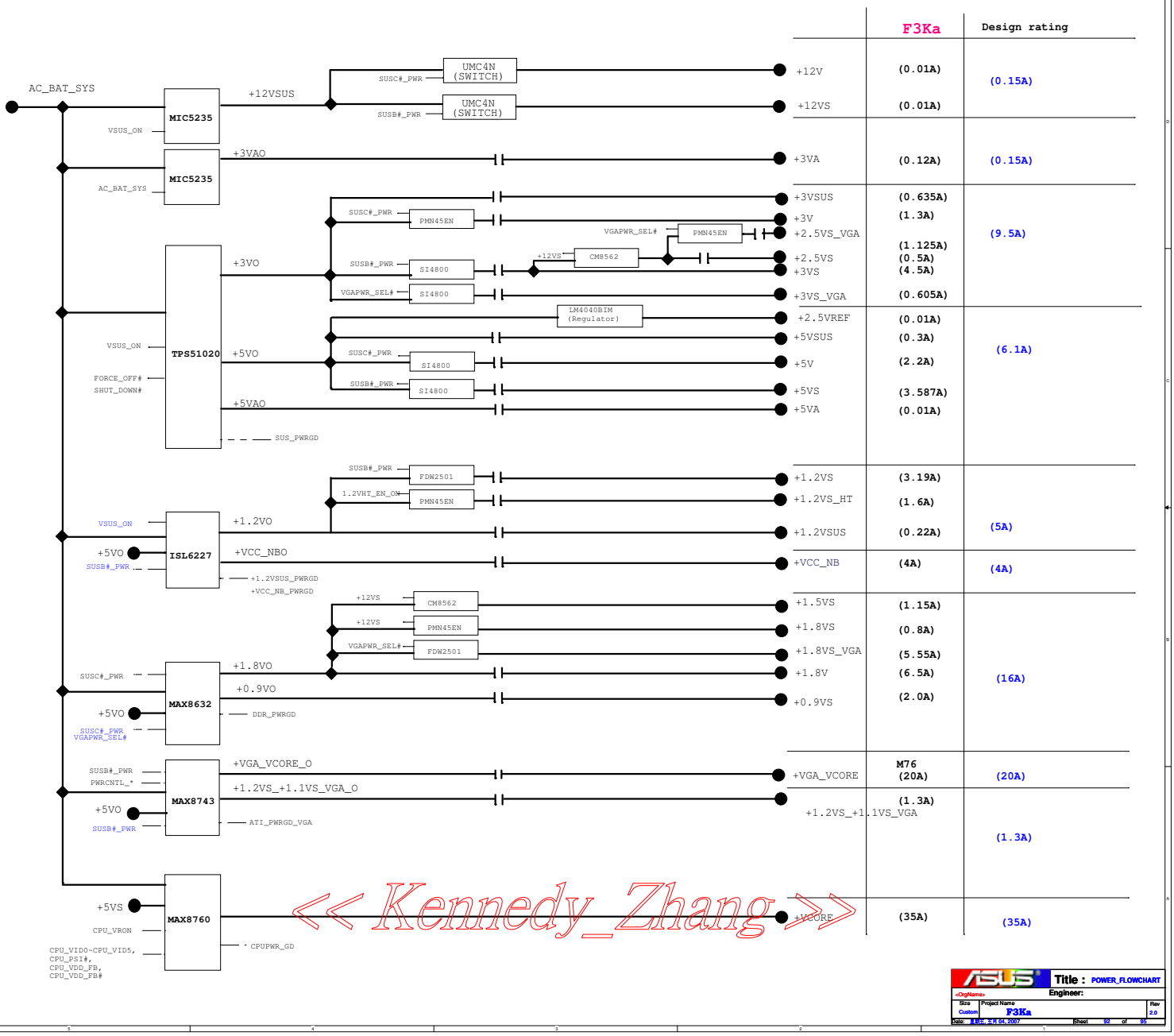


ER_0321-07



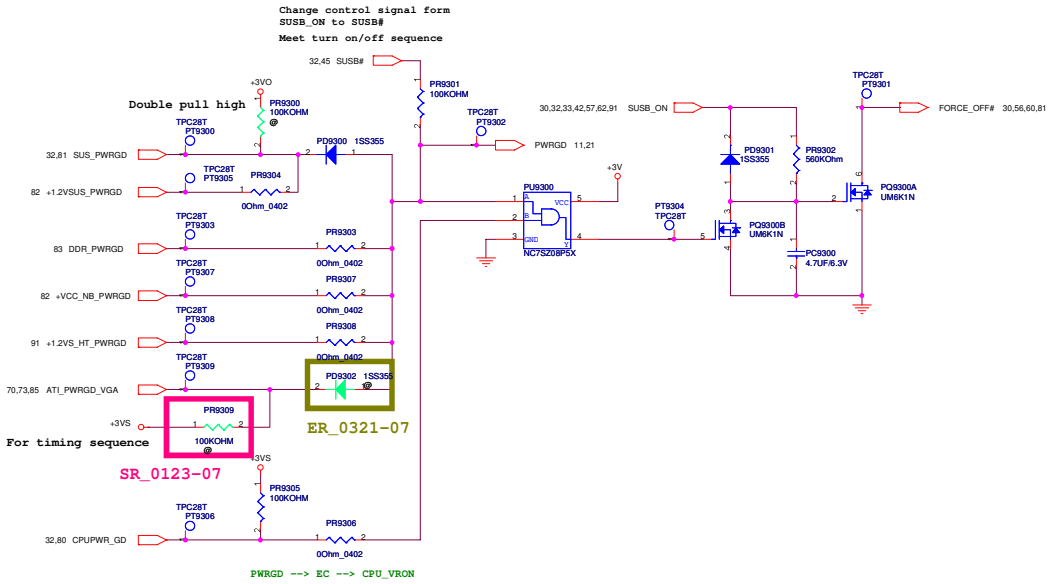
ASUS Title : POWER_LOAD SWITCH
<OrgName> Engineer:
Size: C | Project Name: F3Ka | Rev: 2.0
Date: 星期二, 五月 04, 2007 | Sheet 91 of 95

<< Kennedy_Zhang >>



Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Ka	Rev: 2.0
Date: 星期二, 8 月 04, 2009	Sheet 92 of 95	

POWER GOOD DETECTER



ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Ka	Rev: 2.0
Date: 星期五, 六月 04, 2007	Sheet 83 of 85	

<< Kennedy_Zhang >>

AC_BAT_SYS — AC_BAT_SYS 45,60,80,81,82,83,85,87,88

+3VA — +3VA 3,20,30,32,45,56,62,81,84,90
+5VA — +5VA 81,84

+5VO — +5VO 81,82,83,85,90,91
+3VO — +3VO 81,83,85,91,93
+3VSUS — +3VSUS 3,21,30,32,33,56,57,62,81
+5VSUS — +5VSUS 56,81,87,88,90

+12VSUS — +12VSUS 81,91
+12V — +12V 37,42,52,57,91
+12VS — +12VS 37,45,46,57,84,91

+3V — +3V 21,30,42,45,53,55,57,58,62,84,91,93
+3VS — +3VS 3,7,8,11,12,20,21,29,30,32,33,36,37,40,41,42,45,46,50,51,53,54,55,56,57,58,62,63,70,72,76,86,91,93
+5V — +5V 3,7,45,52,57,58,86,91
+5VS — +5VS 21,30,33,36,37,46,50,51,56,57,76,80,91

+2.5VO — +2.5VO 84,91
+2.5VS — +2.5VS 3,57,84

+1.8VO — +1.8VO 83,84,91
+1.8V — +1.8V 3,5,7,8,57,83
+1.8VS — +1.8VS 3,11,12,20,21,57,76,80,86,91
+0.9V — +0.9V 5,9,57,83

+2.5VREF — +2.5VREF 84,87,88,90
+VCORE — +VCORE 3,5,80

+VGA_VCORE — +VGA_VCORE 57,70,73,85,86
+1.2VS_+1.1VS_VGA — +1.2VS_+1.1VS_VGA 57,70,72,73,85

BAT — BAT 31,88
BAT_CON — BAT_CON 60,88

FOR POWER TEST

+3VA
PJP9400 (SGL_JUMP @) → CPU_VRON_PWR 80
PJP9401 (SGL_JUMP @) — PR9400 1KOhm → SUSB#_PWR 81,82,84,85,91
PJP9402 (SGL_JUMP @) — PR9401 1KOhm → SUSC#_PWR 83,91
PJP9403 (SGL_JUMP @) — PR9402 1KOhm → VSUS_ON 3,30,81,82

Title : POWER_SIGNAL		
<OrgName> Engineer:		
Size: B	Project Name: F3Ka	Rev: 2.0
Date: 星期五, 五月 04, 2007	Sheet 94 of 95	

<< Kennedy_Zhang >>

Title : History

ASUSTek Computer INC. NB1

Engineer:

Size	Project Name	Rev
A	F3Ka	2.0

Date: 星期五, 五月 04, 2007 Sheet 95 of 95

12/08
1. RGB circuits modify
2. p53,54 add common choke
12/11
3. CE5200, CE5203 change_package, USB add power name
4. New card change +3V_PE
5. delete 1 ohm on P76 switch
6. net name IDE_PDASP# -> test point; TVTUNER_ON# pull high to P55; VGND change to GND
7. change power circuits
8. delete L1200, L1203, L1202 and relative power name.
9. unmount R2035 & R2144, change AVDD_SATA's bead to 2A
10. [SB] FANIN[2:0] & TEMPIN2 & VIN0 &VIN[2:7] use 10K to GND
12/12
11. power name +3VS_VGATHEM
12. change R5C833 and unmount C4007
12/13
13. add power name +3VS_CB & +3VS_FP, UIM_PWR_CON
14. swap VRAM
12/14
15. swap DDR, VRAM again
16. follow F3U: Delete R1120, R1121, R1122, R1123, D1100, Q1101, Change U1101 to 74126 to reduce cost
12/15
17. swap DDR
18. Change C2038 to mounting component to meet ATI's requirement
12/16
19. change P11 AVDD to NB_AVDD to prevent short with P83
20. change package: U301, U701, PU8803, X3300, X2001, PU9300, U3602
21. delete 5 unkown line at P74: N17626888, N17631382, N17635879, and 1 power line: N62696617
22. delete another WWAN_MIC+/ WWAN_MIC- port at P36
23. change CE5200 for 6032 package, CE5050 to bigger 11G041210754
24. Q300 Q1100 Q2100 Q5800 change to 07G003000120 for coinsistance
12/20
25. change USB power plane
12/21
26. USB common choke swap (LP3+, 1394) & swap USB 5,6,8
27. follow F3U, Change D5206, D5207, D5208, D5209 to mounting component to Protect the SB USB ports
12/25
28. add C4010 for EMI
12/26
29. swap LPC_AD3, LPC_LDRQ#1 to termination, CLK_CBPCI, LPC_CLK, LPC_CLK_TPM, LPC_CLK_EC to RC
12/27
30. R3701, R3626, C3629 connect to GND_AUDIO
12/30
31. add JP for RGB layout
1/3
32. D4200, R7200 change part
1/5
33. U4100, U5501 change part
34. C400-C403 mount
1/12
35. follow SB 600 errata, change R2022,R2023,R2024 to 680 ohm
36. C3613, C3614 unmount mistake, change to mount part
37. change power circuits

R1.1 2007/01/23
No1: Page21, Strap correction.
No2: Page73, add pull high and change RC value for sequence. and C7300 change X7R
No3: Page70, MEM TD from [0:3] to [3:0]
Page77, change to 7809 because of M76:256MB, M64:128MB
No5: Page31, KB connector inversion.
No6: Page21, follow demo circuits --change to 1uF
Page73, change to 1uF
No8: Page73, follow ref131-5, delete VDDR45 3.3V path & LVDDR 3.3V for M76M, 2.5V for M64M
No9: Page54, unmount R5405 (PCI_RST of WWAN) for 0k function.
No10: Page45, C4502 change to 0.1uF for fixing white screen from CMOS setup. change to 0.22uF
No11: Page20, modify PCI_CLK[3:0] damping R
No12: Page29, SS clock gen will be changed to ICS252 R2949 39.2ohm for M64, R2953 82ohm for M76
No13: Page29, CLK for PCIE_VGA is changed from SRC4 to ATIG1
No14: Page55, unmount R5501 for not supporting TV wake function
No15: Page21 & 55, (For optional)USB7 Use for WLAN & WWAN, USB9 for TVTUNER
No16: Page33, A_RST# to LAN use MOS for leakage issue
No17: Page21 & 55, (For optional) add inverter 2: USB5 use for inverter 1 and inverter 2 and CE4501 change to H=1.1
No18: Page22, USB/ESD diode need mount
No19: Page42, A_RST# to NEW CARD, add diode for leakage issue
No20: Page46, change R4626 & R4627 to 2.7K ohm for CRT detect issue, R4623 & R4624 for DVI function
No21: Page21, change R2107 to 11.3K for USB eye diagram
No22: Page55, change TV TUNER connector and nut lower for thermal issue
No23: Page55, L5502, L4530, RN4505, RN2100 swap
No24: Page21, delete RN2102 because RN4500 does the same function, change branch to page 45
No25: Page50, CE5000 change part for height issue
No26: Page20, modify RTC capacitor = 18pF
No27: Page20, 21, SB600 A21 P/N 02G110012310
R1.2 2007/02/9
No1, Page70, change U7000 to G781-1 and control from EC (unmount R7067, R7068, mount R7064, R7065), VGA_ALARM# connect to EC GPD5
No2, Page40, add R4006(22 ohm) for MDIO9 damping resistor
No3: Page21, CPPE#_DET_B from NEW CARD to SB600 GPM2#
No4, Page70-73, change M76 P/N to A13(02G110014520)
No5: Page20, change R2017 to 499 ohm for ATI suggestion
No6, Page70, Orcad error --> R7009 optional /M76 has symbol error, R5405 & R5501 /X error
No7, Page70, R7048 change to /M76, can't be mounted at M64
No8, Page30, add Force_Off# path to EC reset
No9, Page11,20, follow PowerXpress latest spec, change LVDS_SEL to NB_DFT_GPIO4
Page21, add VGAPWR_SEL to control external power on/off 3/21: Reserve 1K pull high
Page76, DFT_GPIO4 1.8V need to level shift Page76, change LVDS_SEL# power domain : +5VS
No10, Page11, change BACK LIGHT enable pin to BLON pin(follow F3U)
No11, Page36,37, audio amp and relative circuits change
No12, Page70, reserved VGA internal thermal sensor path
Page50, change FAN control circuits
Page30, change EC reset circuits, WATCH_DOG# add test point
No13, Page70-76, for PowerXpress, change +1.8VS, +3VS, +2.5VS to +1.8VS_VGA, +3VS_VGA, +2.5VS_VGA
No14, Page72, for PowerExpress, change RESET circuits, add DIS_VGA_RST# from SB
No15, Page11, add 2 buffer for SMBus, add DDC_CLK_NB/DDC_DAT_NB for DVI, add DACSCL_NB/DACSDA_NB for CRT
Page46, add NB path to CRT and DVI
Page20, add SMBUS_CLK_SEL
No16, Page55, change TV tuner conn. P/N 14G152075002
Page60, DC jack change P/N to 12G145301030
No17, Page11, for DVI HPD, mount R1114 and unmount R1140
No18, Page63, swap finger print usb
No19, Page70, change RN7000 to discrete R, overtemp & alarm connect to +3VS for correct function, delete R7071 & add R5000 pull high to +3VS
No20, unmount R1123, delete R1122 & 036, change DIS_VGA_RST# to VGA_RST#
No21, Page53, add 10pF at BT_DET# for EMI
No22, Page11 delete U1103 and DACSCL_NB is directly drived from NB, change R1128, R1129 to R4606, R4607
No23, delete Ohms: R1100,R1117,R1118,R2011,R2012,R2013,R2021,R2034,R2035,R2113,R2125,R2128,R2130,R2132, R2143,R3011,R3014,R3209,R3301,R3304,R3305,R5311,R5502,R7053
delete no neccessory item: Q3003
No24, Page30, delete R3000 --> JP3003, R3001 --> JP3002, R3010 --> JP3004
Page32, delete R3211 --> JP3203
Page53, delete R5307 --> JP5301, R5308 --> JP5302
No25, Page45, R4526 = 33 ohm, C4502 = 1uF
No26, Page4, follow F3U, change C400-C403 to 2.2pF
R2.0 2007/03/29
No1, Page70, VRAM SIZE strap VGA_GPIO[13:11] changed, vendor table changed
Page70, change memory table
Page75, unmount all B channel for F3Ke
No2, Page29, mount C2918 for EMI
No3, Page57, add 5 discharge circuits for PowerXpress
No4, Page76, reserve LVDS_SEL_18 invertion circuits
No5, Page46, Delete D4620, add Q4603 for HPD polarity reservation (follow F3U)
No6, Page29, reserve U2901 PDTS# to +3VS_VGA for power down when display from internal VGA
No7, Page, change RN to 0603 size
Page, delete colay common choke: L4200, L4523, L4530, L4608, L4609, L4611, L4613, L4614, L6301 L4615, L4616, L5200, L5202, L5204, L5206, L5300, L5301, L5400, L5502
No8, Page55, Change boss footprint
No9, Page70, change RSET from 499 ohm to 549 ohm for RGB EA measurement
No10, Page76, connect to +3VS
No11, Page46, for leakage
No12, Page20, C2025, C2027 change 15pF
No13, Page63, change name : PPCN6300 --> CON6300
No14, Page70, memory size table modified

Post R2.0 2007/04/17
No1, change all 2N7002 to 07G005000214
No2, Page 29, change ICS252 Part No. to 06G011494010
No3, Page 70, change Hynix (16*16) Part No. to 03G151236215
No4, Page 73, modify +3VS_VGA_DELAY timing
No5, Page 11, change Q1100 R1115, and R1116 for fast rising time

R2.0_0504 2007/05/04
No1, For F3Ke PR Hynix VRAM Resistance Strap