

A8J/F SCHEMATIC

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20	ICH7M--CPU, IDE, AUDIO		
21	ICH7M--PCI, PCI-E, USB		
22	ICH7M--GPIO		
23	ICH7M--VCC, GND		
24	HDD & CD-ROM CONN		
25	USB PORTS		
26	SUPER I/O LPC47N217		
27	BIOS & FIR		
28	KBC 38857		
29	SM BUS & POWER PORT		
30	PCI-E--GIGA_LAN RTL8111B		
31	PCI-E--MINI_CARD		
32	PCI-E--NEW_CARD		
33	PCI--1394, CardReader R5C832		
34	PCI--4 IN1 CON		
35	PCI--Empty		
36	AUDIO CODEC AD1986A		
37	AUDIO AMP G1420		
38	MDC, B/T, TPM & DISCHG, HOLE		
39	DVI CONN		
40	ACIN, BAT, FAN, I/O PORT		
41	SW & LED & TP		
42	POWER-ON SEQUENCE		
43	HISTORY		
44	I/O PORT		

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PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Integrated LAN	AD24(NO USE)			
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
 CLK_GEN. = 1101001x (D2h)
 DDR_SODIMMO = 1010000x (A0h)
 DDR_SODIMM1 = 1010010x (A4h)
 VGA_Thermal IC = 1001100x (9Ah)

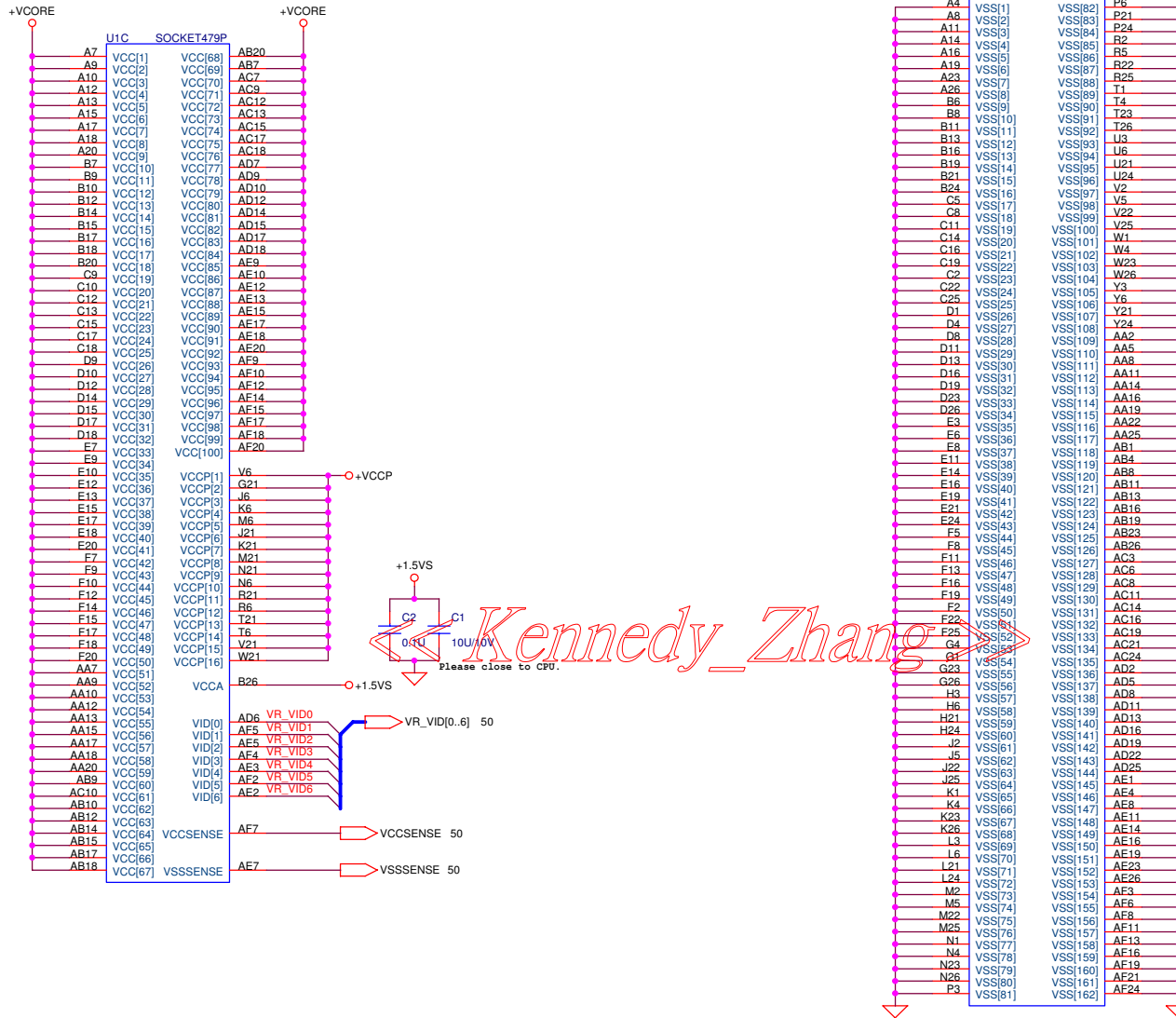
ICH7M_GPIO	Use As	Signal Name	Power	
GPIO 00	i	GPI	PM_BMBUSY#	+3VS
GPIO 01	i	GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i	GPO	BACK_OFF#	+3VS
GPIO 07	i	GPI	RF_SW_OFF#	+3VS
GPIO 08	i	GPI	EXTSMI#_3A	+3VSUS
GPIO 09	i	GPI	PD_DET#	+3VSUS
GPIO 10	i	GPI	CHG_FULL_OC	+3VSUS
GPIO 11	i	Native	SMB_ALERT#	+3VSUS
GPIO 12	i	GPI	KB_SCI#	+3VSUS
GPIO 13	i	GPI	SIO_SMI#	+3VSUS
GPIO 14	i	GPI	PD_UnDock#(PWRLMT#)	+3VSUS
GPIO 15	i	GPO	802_LED_EN#	+3VSUS
GPIO 16	00	GPO	PM_DPRSPLPVR	+3VS
GPIO 17	01	GPO	PCI_GNT#5	+3VS
GPIO 18	01	GPO	STP_PCI#	+3VS
GPIO 19	i1	GPI	PD_RDY#	+3VS
GPIO 20	01	GPO	STP_CPU#	+3VS
GPIO 21	i1	GPO	PD_SIO_RST#	+3VS
GPIO 22	i1	Native	PCI_REQ#4	+3VS
GPIO 23	i1	Native	LPC_DRQ#1	+3VS
GPIO 24	00	GPO	PD_EN#	+3VSUS
GPIO 25	01	GPO	CB_SD#	+3VSUS
GPIO 26	00	GPO	OP_SD#	+3VSUS
GPIO 27	00	GPO	WLAN_ON#	+3VSUS
GPIO 28	00	GPO	1Hz	+3VSUS
GPIO 29	i0	Native	USB_OC#5	+3VSUS
GPIO 30	i0	Native	USB_OC#6	+3VSUS
GPIO 31	i0	Native	USB_OC#7	+3VSUS
GPIO 32	01	GPO	PM_CLKRUN#	+3VS
GPIO 33	01	GPO	BT_ON/OFF#	+3VS
GPIO 34	00	GPO	FWH_WP#	+3VS
GPIO 35	00	GPO	SATACLKREQ#	+3VS
GPIO 36	i0	GPO	BT_LED_EN#	+3VS
GPIO 37	i0	GPI	PCB_ID0	+3VS
GPIO 38	i0	GPI	PCB_ID1	+3VS
GPIO 39	i0	GPI	PCB_ID2	+3VS
GPIO [40:47]	NA	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS	
GPIO 49	Native	H_PWRGD	+VCORE	

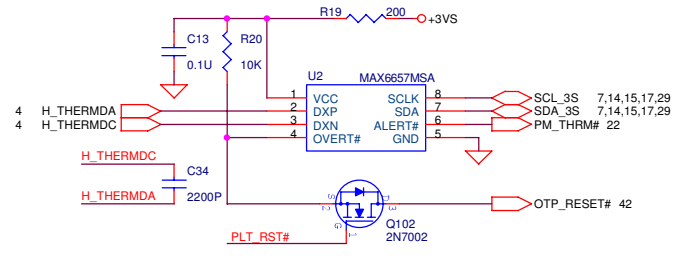
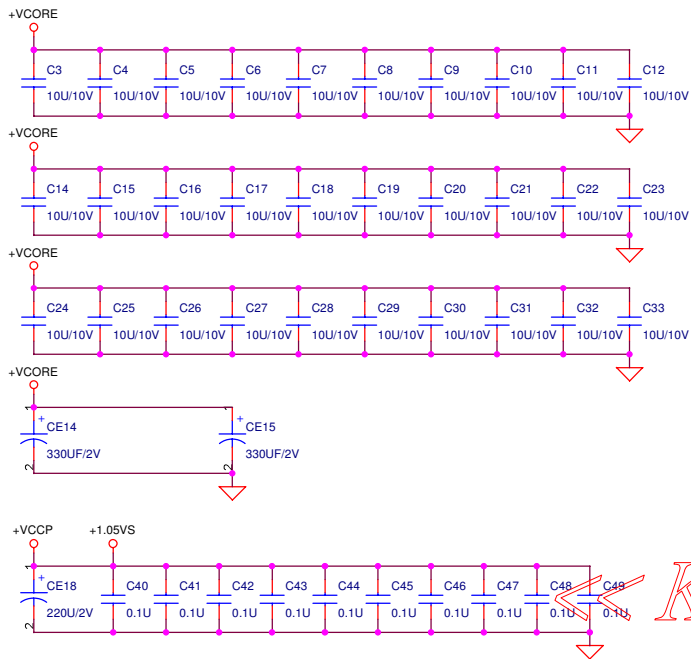
M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DP	+3V
P57	GPO	ADD_B1	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

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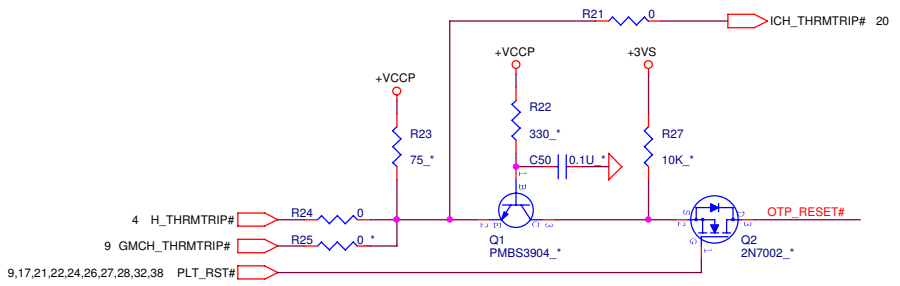
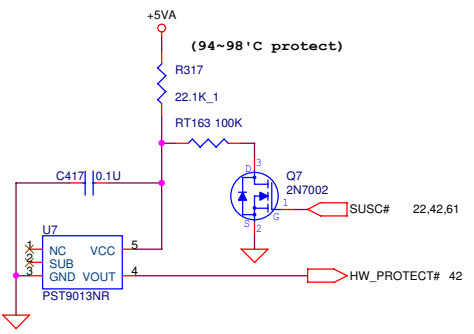
47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI	NONE	+3VS
GPIO11	GPO	NONE	+3VS
GPIO12	GPO	NONE	+3VS
GPIO13	GPI	NONE	+3VS
GPIO14	GPI	NONE	+3VS
GPIO23	GPO	ATI_RST#	+3VS
GPIO40	GPI		+3VS
GPIO41	GPI		+3VS
GPIO40	GPI		+3VS
GPIO43	GPI		+3VS
GPIO44	GPI		+3VS
GPIO45	GPI		+3VS
GPIO46	GPI	VGA_DETEC#	+3VS
GPIO47	GPI		+3VS

+VCCP +VCCP 4,6,8,11,12,20,23,52
 +1.5VS +1.5VS 9,11,12,17,23,31,32,38,52
 +VCORE +VCORE 6,50





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+VCCP	4,5,8,11,12,20,23,52
+VCORE	5,50
+3VS	7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+5VA	51,54

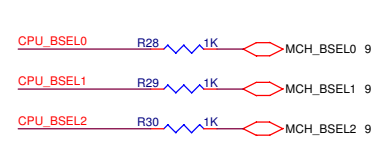
ASUSTek COMPUTER INC.

4 FL, No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

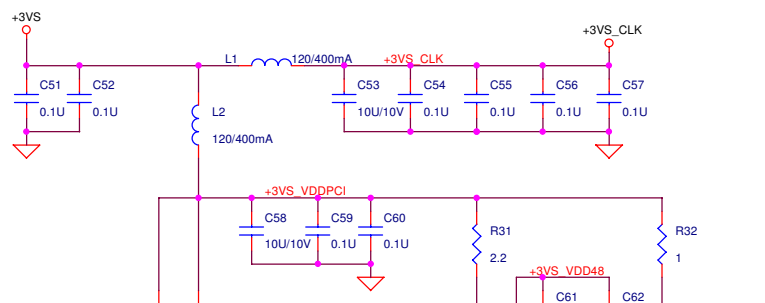
Title: **CPU CAP, THERMAL SENSOR**

Size	Document Number	Rev
Custom	A8J/F	2.0

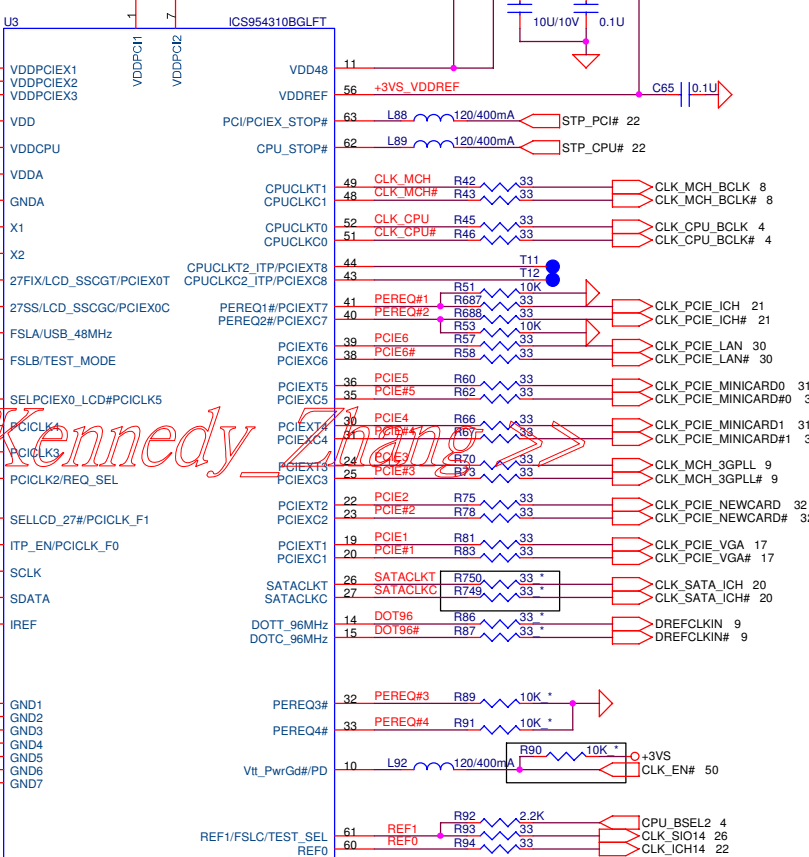
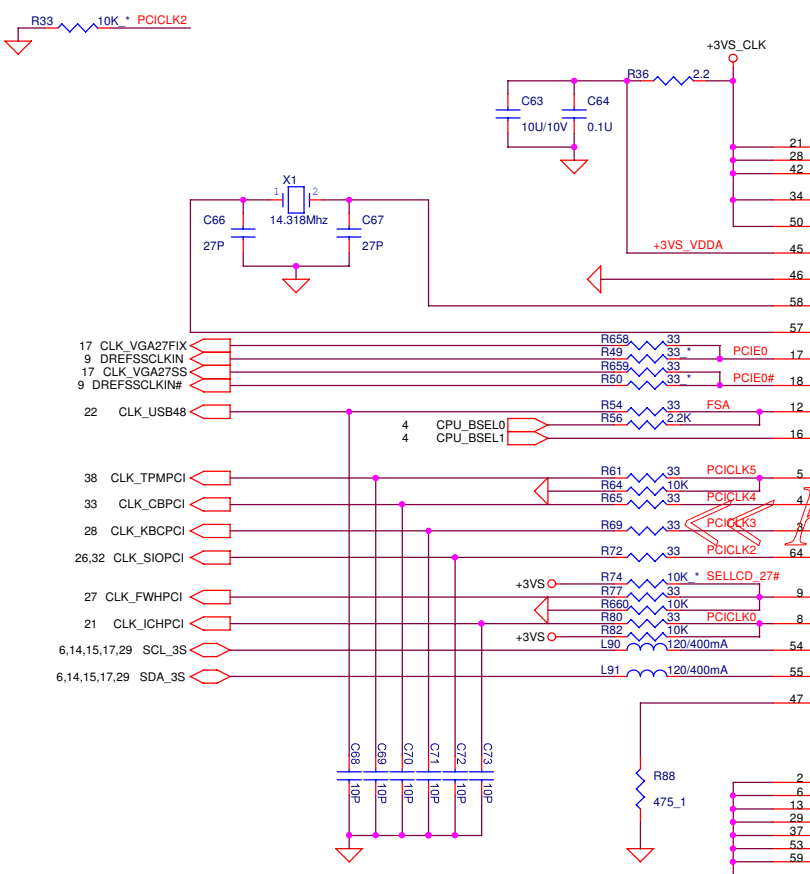
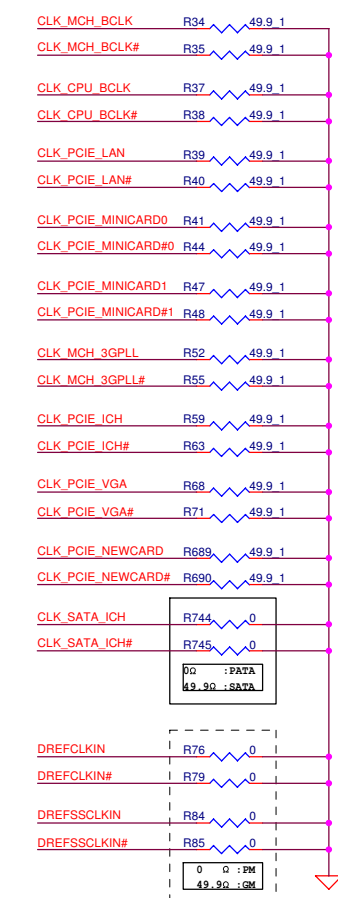
Date: Wednesday, March 29, 2006 Sheet 6 of 63



Bclk	FSB	FSLC	FSLB	FSLA
133	533	L	L	H
166	667	L	H	H



PLACE termination close to source IC

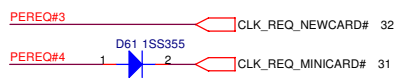


/	PIN9	PIN5	PIN17	PIN18
*	0	X	27FIX	27SS
	1	0	96MSS_T	96MSS_C
	1	1	PCIEX0_T	PCIEX0_C

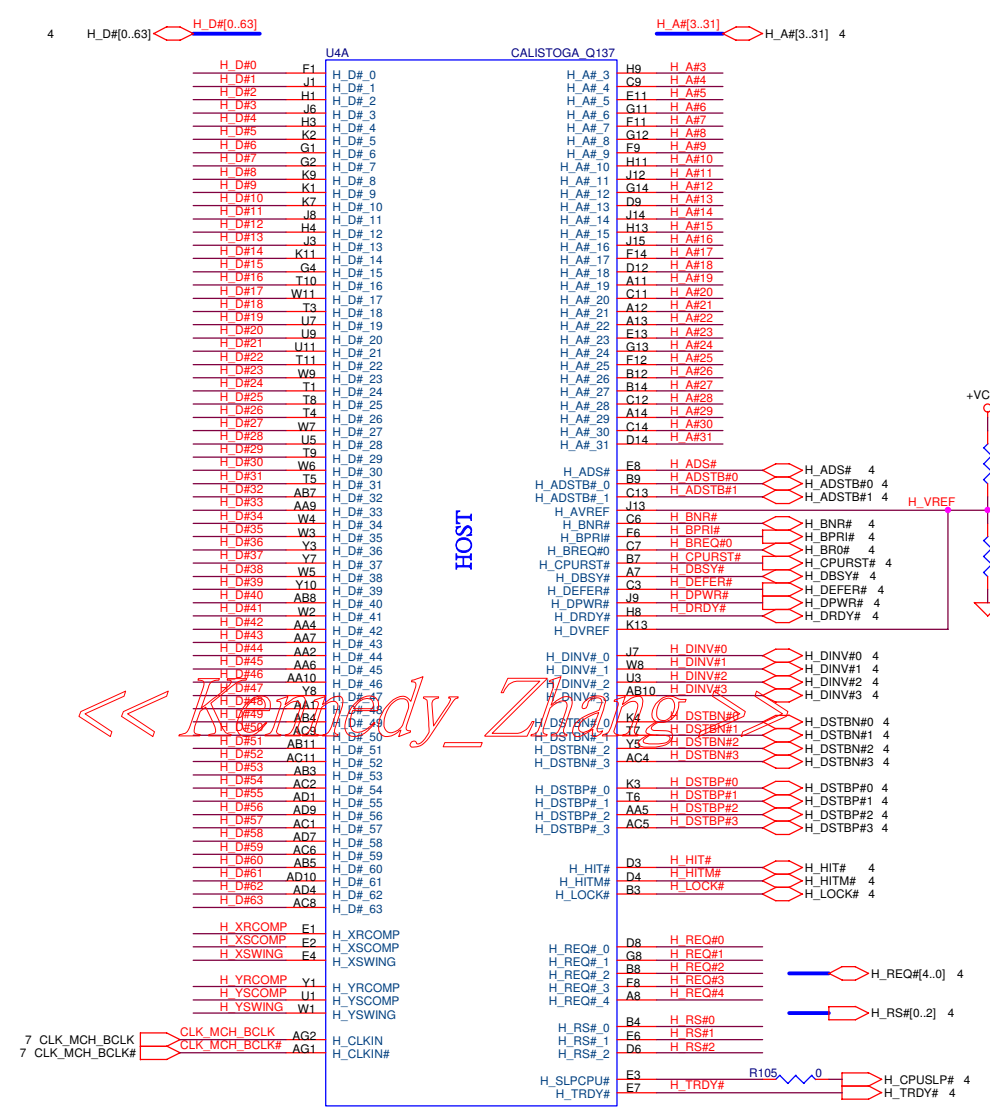
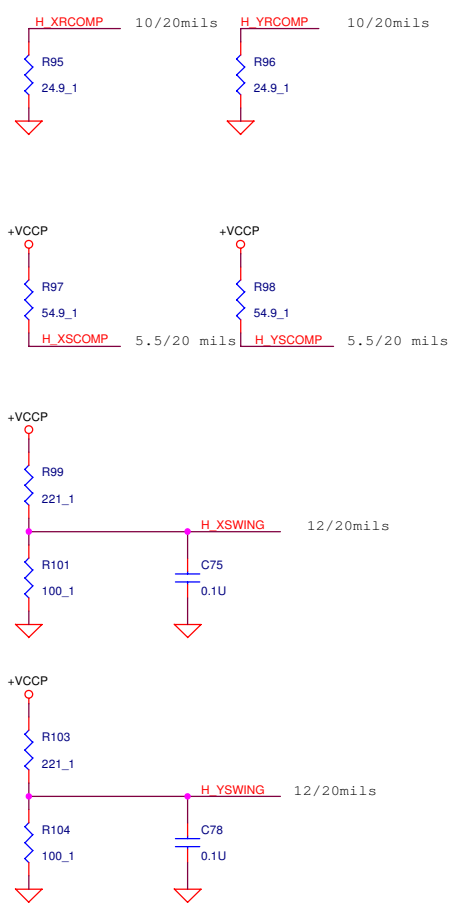
PIN8 : 0=SRC Pair, 1=CPU_ITP pair
 PIN64: 0=PCIEXCLK, 1=PEREQ#

Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
 Int. PD: PIN64

PEREQ#1: PCIEX0, PCIEX6
 PEREQ#2: PCIEX1, PCIEX8
 PEREQ#3: PCIEX2, PCIEX4
 PEREQ#4: PCIEX3, PCIEX5, PCIEX7



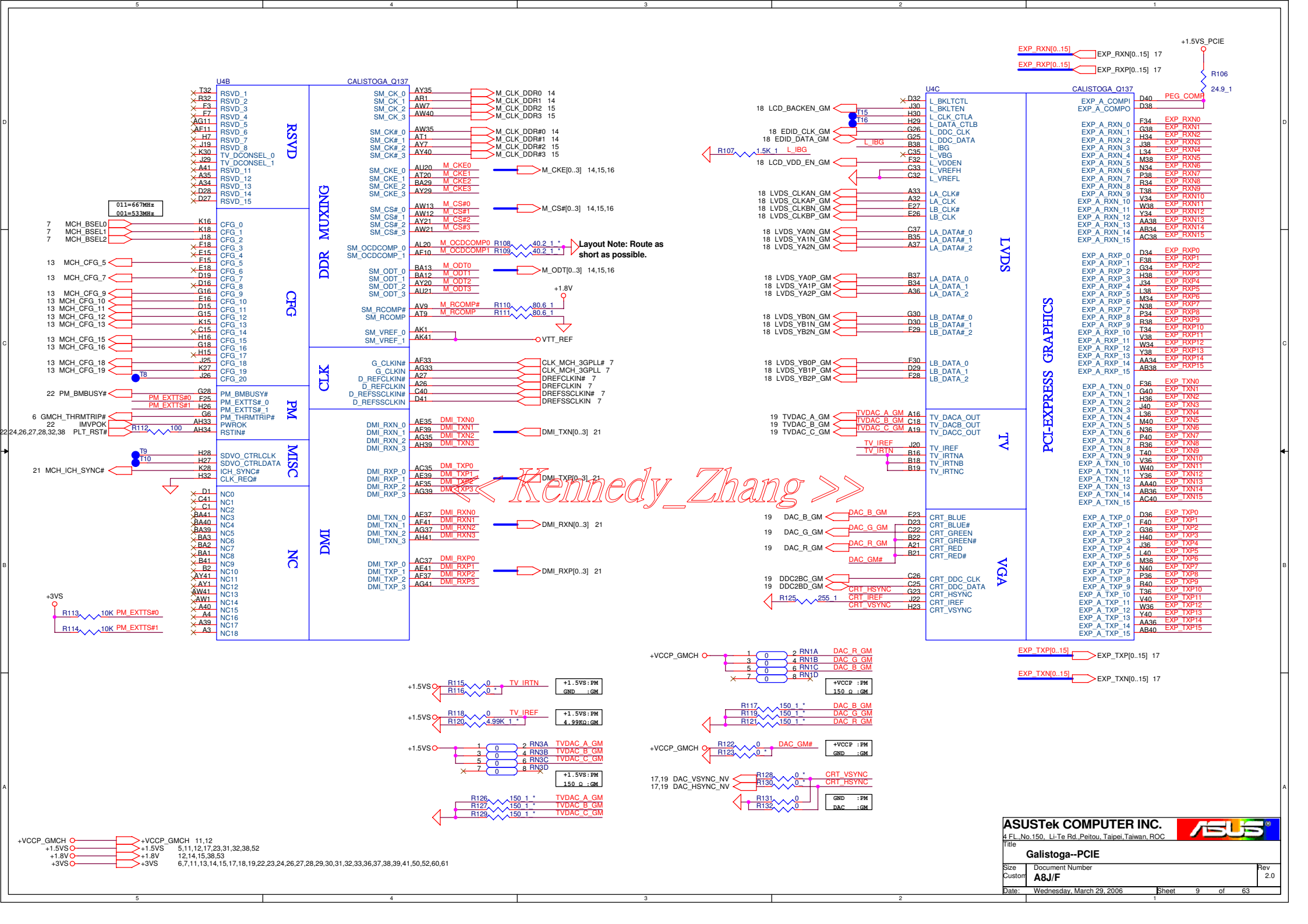
+3VS → +3VS 6,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61



+VCCP \rightarrow +VCCP 4,5,6,11,12,20,23,52

<500 mil (55 Ohm)
T/B trace 5.5,
Space 25

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011=667MHz
001=533MHz

+VCCP_GMCH	+VCCP_GMCH	11,12
+1.5VS	+1.5VS	5,11,12,17,23,31,32,38,52
+1.8V	+1.8V	12,14,15,38,53
+3VS	+3VS	6,7,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61

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14 M_A_DQ[0..63]

M_A_D00	AJ35	SA_D00
M_A_D01	AJ34	SA_D01
M_A_D02	AM31	SA_D02
M_A_D03	AM31	SA_D03
M_A_D04	AM33	SA_D04
M_A_D05	AJ38	SA_D05
M_A_D06	AJ32	SA_D06
M_A_D07	AH31	SA_D07
M_A_D08	AN35	SA_D08
M_A_D09	AP33	SA_D09
M_A_D010	AB31	SA_D010
M_A_D011	AP31	SA_D011
M_A_D012	AN38	SA_D012
M_A_D013	AM36	SA_D013
M_A_D014	AM34	SA_D014
M_A_D015	AN33	SA_D015
M_A_D016	AK26	SA_D016
M_A_D017	AL27	SA_D017
M_A_D018	AM26	SA_D018
M_A_D019	AN24	SA_D019
M_A_D020	AK28	SA_D020
M_A_D021	AL28	SA_D021
M_A_D022	AM24	SA_D022
M_A_D023	AP28	SA_D023
M_A_D024	AP23	SA_D024
M_A_D025	AL22	SA_D025
M_A_D026	AP21	SA_D026
M_A_D027	AN20	SA_D027
M_A_D028	AL23	SA_D028
M_A_D029	AP24	SA_D029
M_A_D030	AP20	SA_D030
M_A_D031	AT21	SA_D031
M_A_D032	AR12	SA_D032
M_A_D033	AR14	SA_D033
M_A_D034	AP13	SA_D034
M_A_D035	AP12	SA_D035
M_A_D036	AT13	SA_D036
M_A_D037	AT12	SA_D037
M_A_D038	AL14	SA_D038
M_A_D039	AL12	SA_D039
M_A_D040	AK9	SA_D040
M_A_D041	AN7	SA_D041
M_A_D042	AK8	SA_D042
M_A_D043	AK7	SA_D043
M_A_D044	AP9	SA_D044
M_A_D045	AN9	SA_D045
M_A_D046	AT5	SA_D046
M_A_D047	AL5	SA_D047
M_A_D048	AY2	SA_D048
M_A_D049	AW2	SA_D049
M_A_D050	AP1	SA_D050
M_A_D051	AN2	SA_D051
M_A_D052	AV2	SA_D052
M_A_D053	AT3	SA_D053
M_A_D054	AN1	SA_D054
M_A_D055	AL2	SA_D055
M_A_D056	AG7	SA_D056
M_A_D057	AF9	SA_D057
M_A_D058	AG4	SA_D058
M_A_D059	AG9	SA_D059
M_A_D060	AH6	SA_D060
M_A_D061	AF4	SA_D061
M_A_D062	AF4	SA_D062
M_A_D063	AF8	SA_D063

DDR SYSTEM MEMORY A

CALISTOGA_Q137	AU12	M_A_BS#0 14,16
	AV14	M_A_BS#1 14,16
	BA20	M_A_BS#2 14,16
		M_A_CAS# 14,16
	AY19	
SA_CAS#	AJ33	M_A_DM0
SA_DM_0	AM35	M_A_DM1
SA_DM_1	AL26	M_A_DM2
SA_DM_2	AN22	M_A_DM3
SA_DM_3	AM14	M_A_DM4
SA_DM_4	AL9	M_A_DM5
SA_DM_5	AR3	M_A_DM6
SA_DM_6	AH4	M_A_DM7
SA_DM_7		
SA_DOS_0	AK33	M_A_DOS0
SA_DOS_1	AT33	M_A_DOS1
SA_DOS_2	AN28	M_A_DOS2
SA_DOS_3	AM22	M_A_DOS3
SA_DOS_4	AN12	M_A_DOS4
SA_DOS_5	AN8	M_A_DOS5
SA_DOS_6	AP3	M_A_DOS6
SA_DOS_7	AG5	M_A_DOS7
SA_DOS#_0	AK32	M_A_DOS#0
SA_DOS#_1	AN27	M_A_DOS#1
SA_DOS#_2	AM21	M_A_DOS#2
SA_DOS#_3	AM12	M_A_DOS#3
SA_DOS#_4	AL8	M_A_DOS#4
SA_DOS#_5	AN3	M_A_DOS#5
SA_DOS#_6	AH5	M_A_DOS#6
SA_DOS#_7		
SA_MA_0	AY16	M_A_A0
SA_MA_1	AU14	M_A_A1
SA_MA_2	AW16	M_A_A2
SA_MA_3	BA16	M_A_A3
SA_MA_4	BA17	M_A_A4
SA_MA_5	AU16	M_A_A5
SA_MA_6	AV17	M_A_A6
SA_MA_7	AU17	M_A_A7
SA_MA_8	AW17	M_A_A8
SA_MA_9	AT16	M_A_A9
SA_MA_10	AU13	M_A_A10
SA_MA_11	AT17	M_A_A11
SA_MA_12	AV20	M_A_A12
SA_MA_13	AV12	M_A_A13
SA_RAS#	AW14	T17
SA_RCVENIN#	AK23	T19
SA_RCVENOUT#	AK24	T19
SA_WE#	AY14	

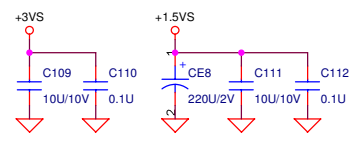
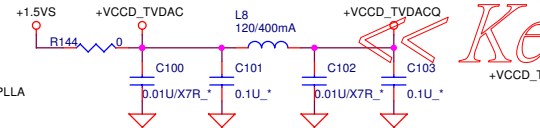
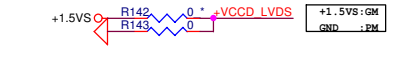
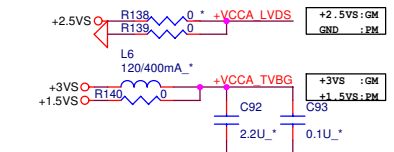
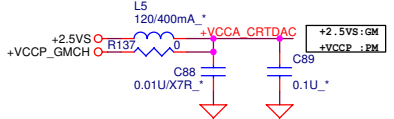
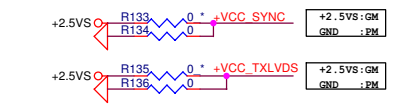
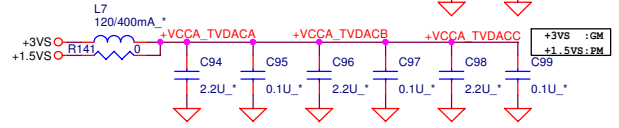
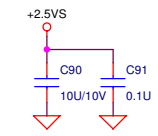
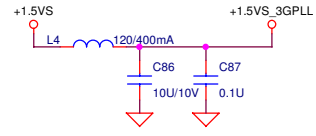
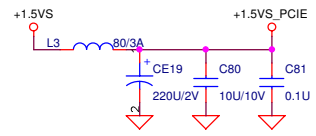
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15 M_B_DQ[0..63]

M_B_D00	AK39	SB_D00
M_B_D01	AJ37	SB_D01
M_B_D02	AP39	SB_D02
M_B_D03	AP41	SB_D03
M_B_D04	AP41	SB_D04
M_B_D05	AJ38	SB_D05
M_B_D06	AN41	SB_D06
M_B_D07	AP41	SB_D07
M_B_D08	AT40	SB_D08
M_B_D09	AV41	SB_D09
M_B_D010	AU38	SB_D010
M_B_D011	AV38	SB_D011
M_B_D012	AP38	SB_D012
M_B_D013	AR40	SB_D013
M_B_D014	AW38	SB_D014
M_B_D015	AY38	SB_D015
M_B_D016	BA38	SB_D016
M_B_D017	AV36	SB_D017
M_B_D018	AR36	SB_D018
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M_B_D020	BA36	SB_D020
M_B_D021	AU36	SB_D021
M_B_D022	AP33	SB_D022
M_B_D023	AP33	SB_D023
M_B_D024	AY33	SB_D024
M_B_D025	BA33	SB_D025
M_B_D026	AT31	SB_D026
M_B_D027	AU29	SB_D027
M_B_D028	AU31	SB_D028
M_B_D029	AW31	SB_D029
M_B_D030	AV29	SB_D030
M_B_D031	AW29	SB_D031
M_B_D032	AM19	SB_D032
M_B_D033	AL19	SB_D033
M_B_D034	AP14	SB_D034
M_B_D035	AN14	SB_D035
M_B_D036	AM17	SB_D036
M_B_D037	AM16	SB_D037
M_B_D038	AP15	SB_D038
M_B_D039	AK15	SB_D039
M_B_D040	AK17	SB_D040
M_B_D041	AK10	SB_D041
M_B_D042	AI9	SB_D042
M_B_D043	AN10	SB_D043
M_B_D044	AK13	SB_D044
M_B_D045	AP34	SB_D045
M_B_D046	AH11	SB_D046
M_B_D047	AK10	SB_D047
M_B_D048	AJ8	SB_D048
M_B_D049	AW10	SB_D049
M_B_D050	BA4	SB_D050
M_B_D051	AW4	SB_D051
M_B_D052	AY9	SB_D052
M_B_D053	AY9	SB_D053
M_B_D054	AW5	SB_D054
M_B_D055	AY5	SB_D055
M_B_D056	AV4	SB_D056
M_B_D057	AR5	SB_D057
M_B_D058	AK4	SB_D058
M_B_D059	AK3	SB_D059
M_B_D060	AT4	SB_D060
M_B_D061	AK5	SB_D061
M_B_D062	AJ5	SB_D062
M_B_D063	AJ3	SB_D063

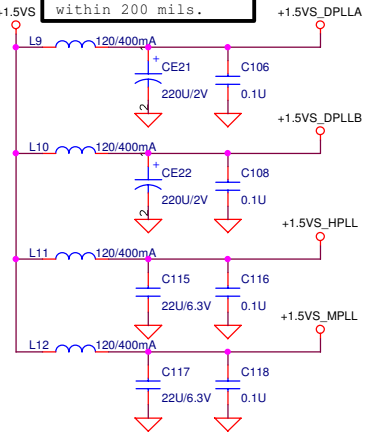
DDR SYSTEM MEMORY B

CALISTOGA_Q137	AT24	M_B_BS#0 15,16
	AV23	M_B_BS#1 15,16
	AY28	M_B_BS#2 15,16
		M_B_CAS# 15,16
	AR24	M_B_DM0
SB_CAS#	AK36	M_B_DM1
SB_DM_0	AR38	M_B_DM2
SB_DM_1	AT36	M_B_DM3
SB_DM_2	BA31	M_B_DM4
SB_DM_3	AL17	M_B_DM5
SB_DM_4	AH8	M_B_DM6
SB_DM_5	BA5	M_B_DM7
SB_DM_6	AN4	M_B_DM7
SB_DM_7		
SB_DOS_0	AM39	M_B_DOS0
SB_DOS_1	AT39	M_B_DOS1
SB_DOS_2	AU35	M_B_DOS2
SB_DOS_3	AR29	M_B_DOS3
SB_DOS_4	AR16	M_B_DOS4
SB_DOS_5	AR10	M_B_DOS5
SB_DOS_6	AR7	M_B_DOS6
SB_DOS_7	AN5	M_B_DOS7
SB_DOS#_0	AM40	M_B_DOS#0
SB_DOS#_1	AU39	M_B_DOS#1
SB_DOS#_2	AT35	M_B_DOS#2
SB_DOS#_3	AP29	M_B_DOS#3
SB_DOS#_4	AP16	M_B_DOS#4
SB_DOS#_5	AT10	M_B_DOS#5
SB_DOS#_6	AT7	M_B_DOS#6
SB_DOS#_7	AP5	M_B_DOS#7
SB_MA_0	AY23	M_B_A0
SB_MA_1	AW24	M_B_A1
SB_MA_2	AY24	M_B_A2
SB_MA_3	AR28	M_B_A3
SB_MA_4	AT27	M_B_A4
SB_MA_5	AT28	M_B_A5
SB_MA_6	AU27	M_B_A6
SB_MA_7	AV28	M_B_A7
SB_MA_8	AW27	M_B_A8
SB_MA_9	AW27	M_B_A9
SB_MA_10	AV24	M_B_A10
SB_MA_11	BA27	M_B_A11
SB_MA_12	AY27	M_B_A12
SB_MA_13	AR23	M_B_A13
SB_RAS#	AU23	T18
SB_RCVENIN#	AK18	T20
SB_RCVENOUT#	AK18	T20
SB_WE#	AR27	

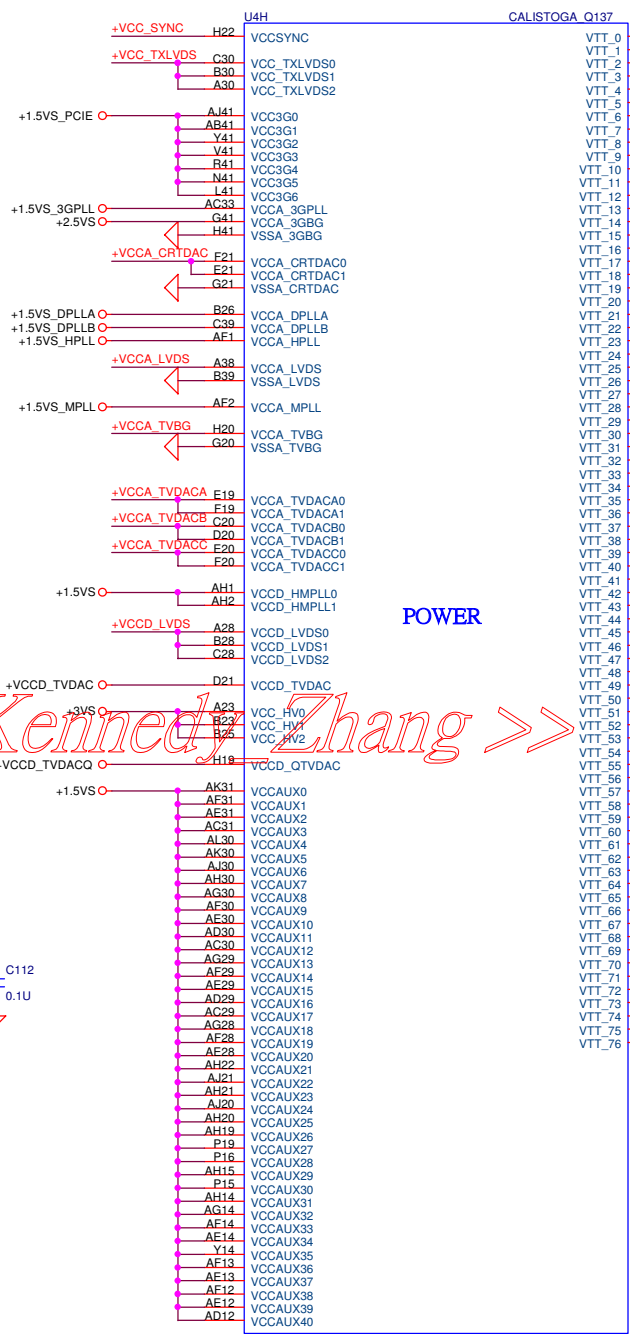


NOTE: 0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

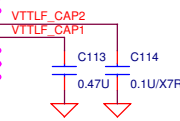
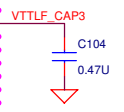
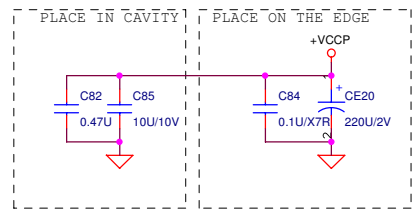


+1.5VS	5,9,12,17,23,31,32,38,52
+2.5VS	17,19,38,54
+3VS	6,7,9,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+VCCP	4,5,6,8,12,20,23,52



POWER

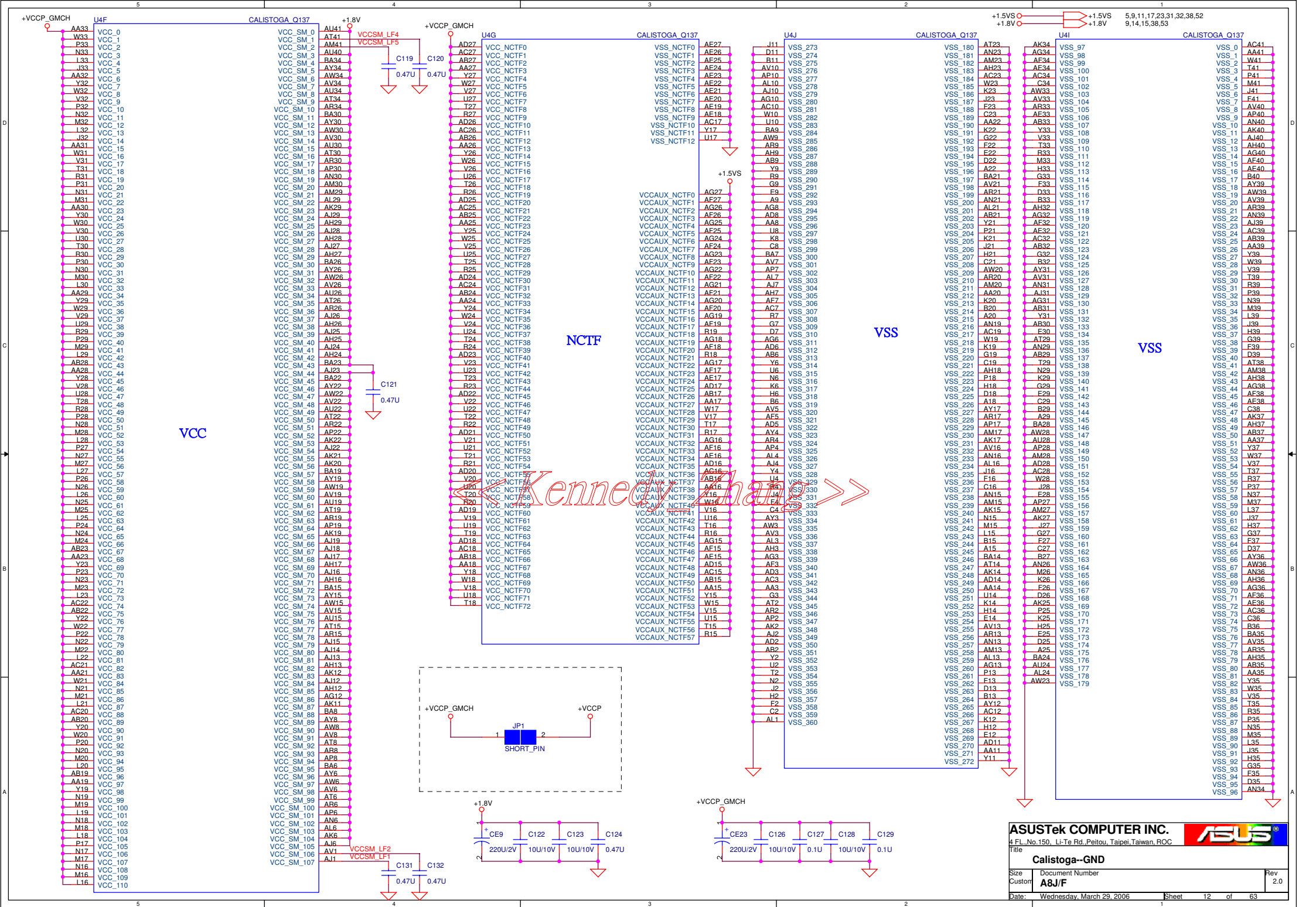
<< Kennedy Zhang >>



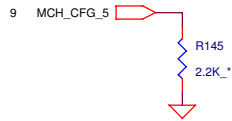
ASUSTek COMPUTER INC.

4 FL, No. 150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

Title		
Calistoga--PWR		
Size	Document Number	Rev
Custom	A8/JF	2.0
Date:	Wednesday, March 29, 2006	Sheet 11 of 63

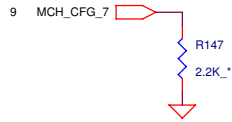


ASUSTek COMPUTER INC.			
4 FL No. 150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC			
Title			
Calistoga--GND			
Size	Document Number		Rev
Custom	A8/JF		2.0
Date:	Wednesday, March 29, 2006	Sheet	12 of 63



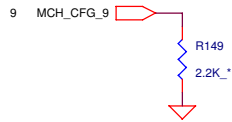
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



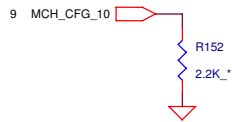
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



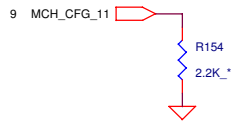
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

LOW = RESERVED
HIGH = MOBILITY (Default)

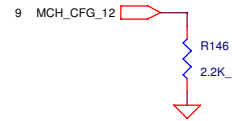


CFG11 : PSB 4x CLK ENABLE

LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

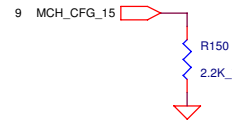
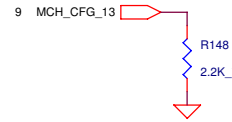
CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.

+3VS 6,7,9,11,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61



CFG[13:12] : GMCH TEST MODE SELECT

00 = Partial CLK gating disable
 01 = XOR Mode Enable
 10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)



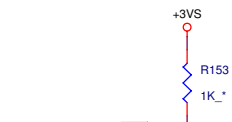
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
 HIGH = 1.5V

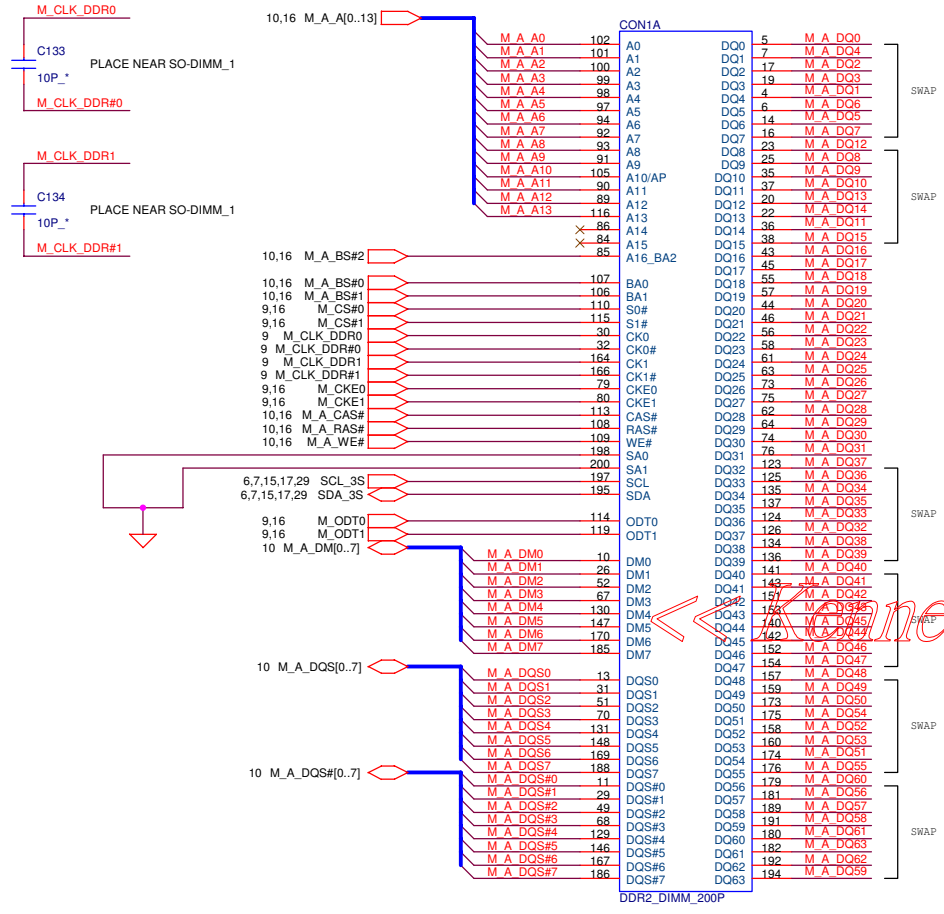


CFG19 : DMI LANE REVERSAL

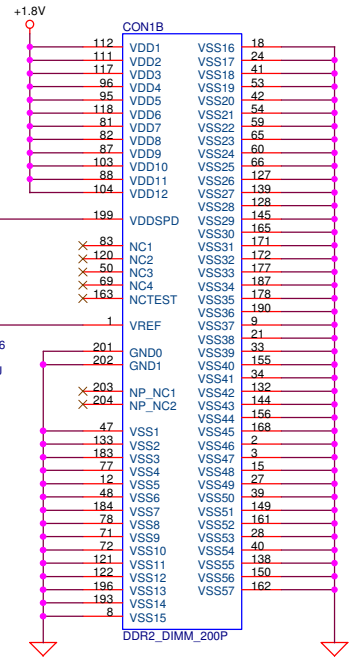
LOW = NORMAL (Default)
 HIGH = LANES REVERSED

+1.8V \rightarrow +1.8V
 +3VS \rightarrow +3VS
 9,12,15,38,53
 6,7,9,11,13,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61

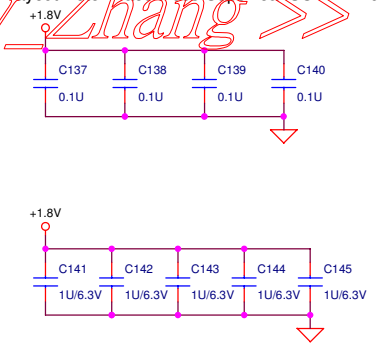
10 M_A_DQ[0..63] \rightarrow M_A_DQ[0..63]

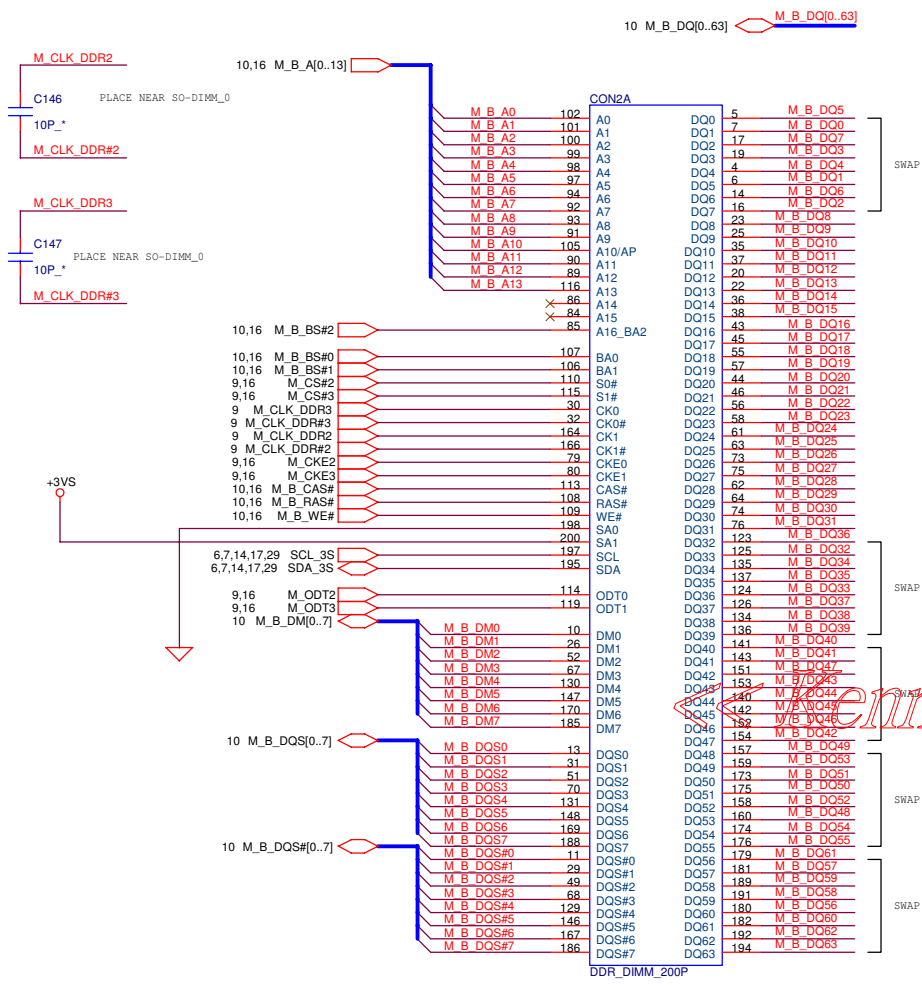


SWAP
 SWAP
 SWAP
 SWAP
 SWAP
 SWAP
 SWAP



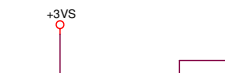
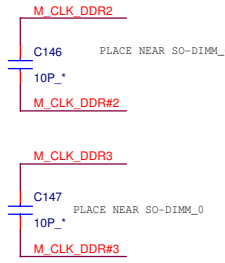
Layout Note: Place these Caps near SO-DIMM 0
 << Medy Zhang >>



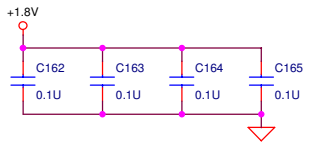


+1.8V → +1.8V
 +3VS → +3VS
 +5V → +5V

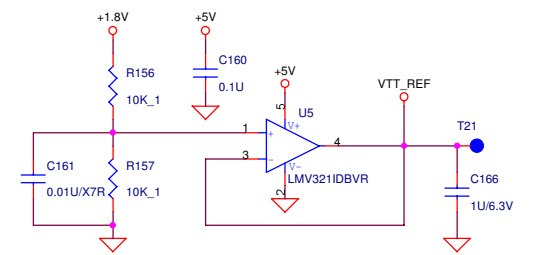
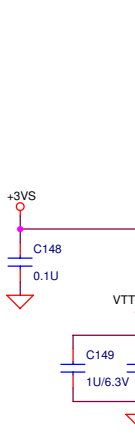
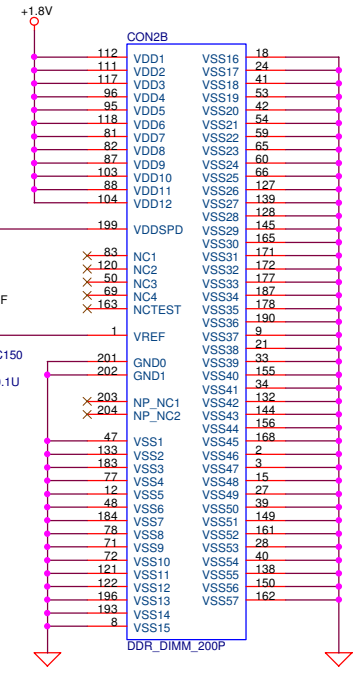
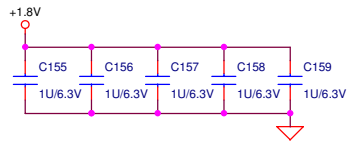
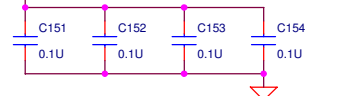
9,12,14,38,53
 6,7,9,11,13,14,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
 17,19,25,28,32,36,38,40,41,59,61

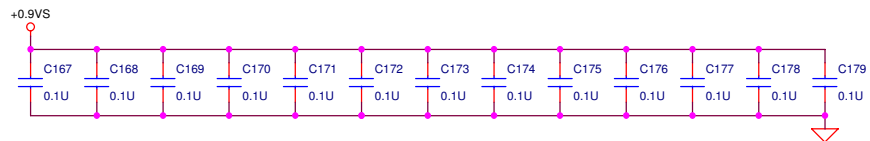


Layout Note: Place these High-Freq decoupling Caps near the GMCH

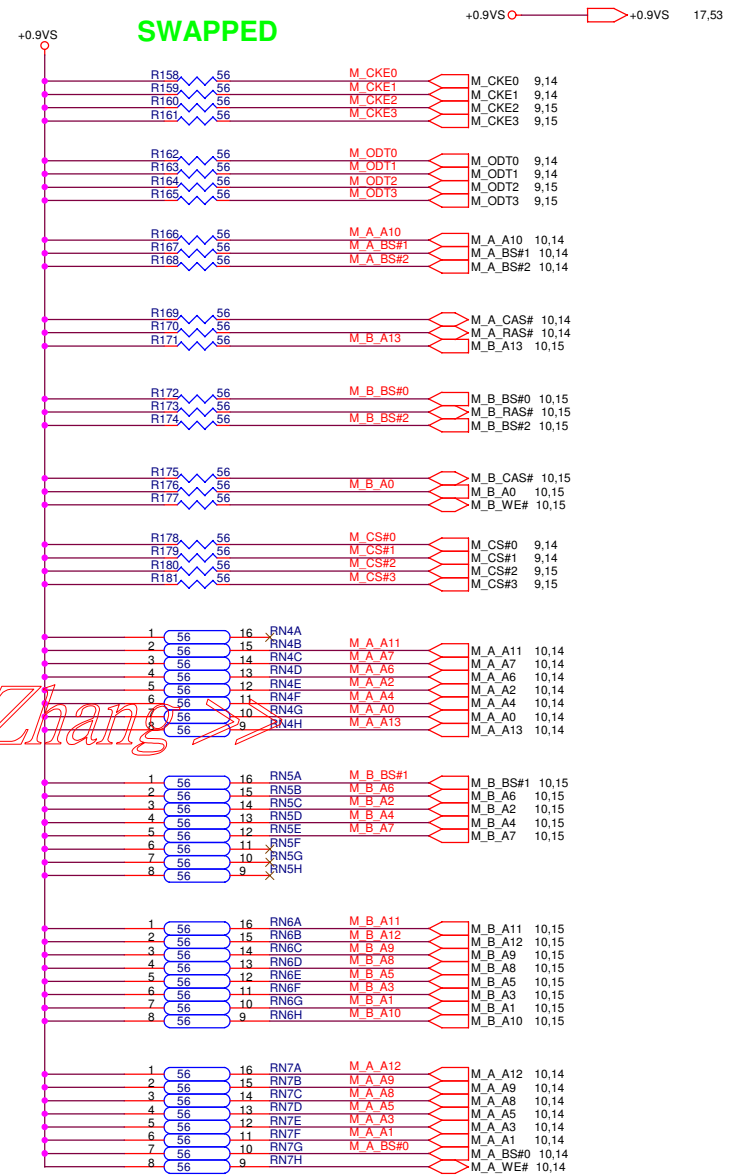
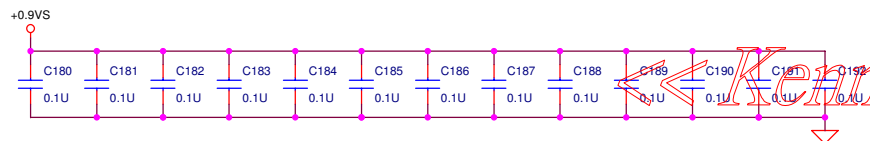


Layout Note: Place these Caps near SO DIMM 0

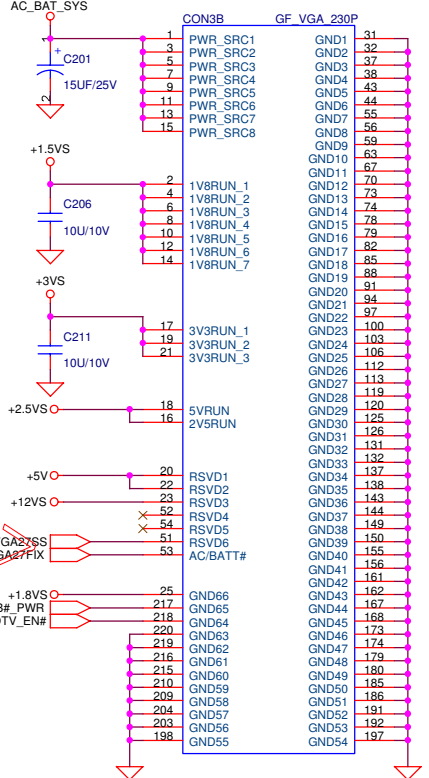
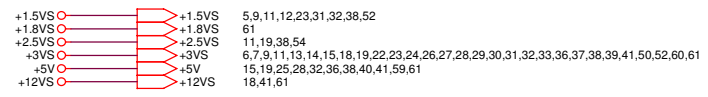
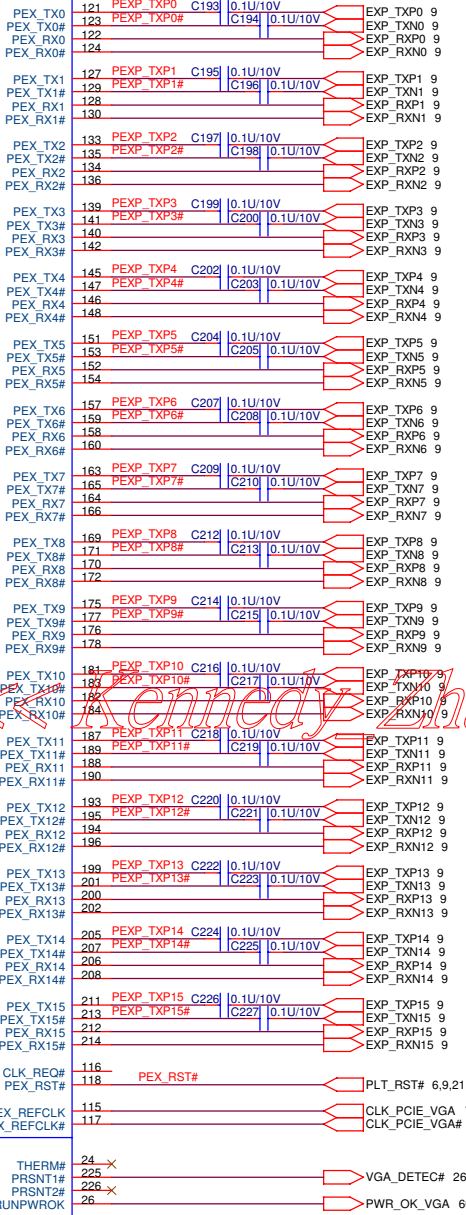
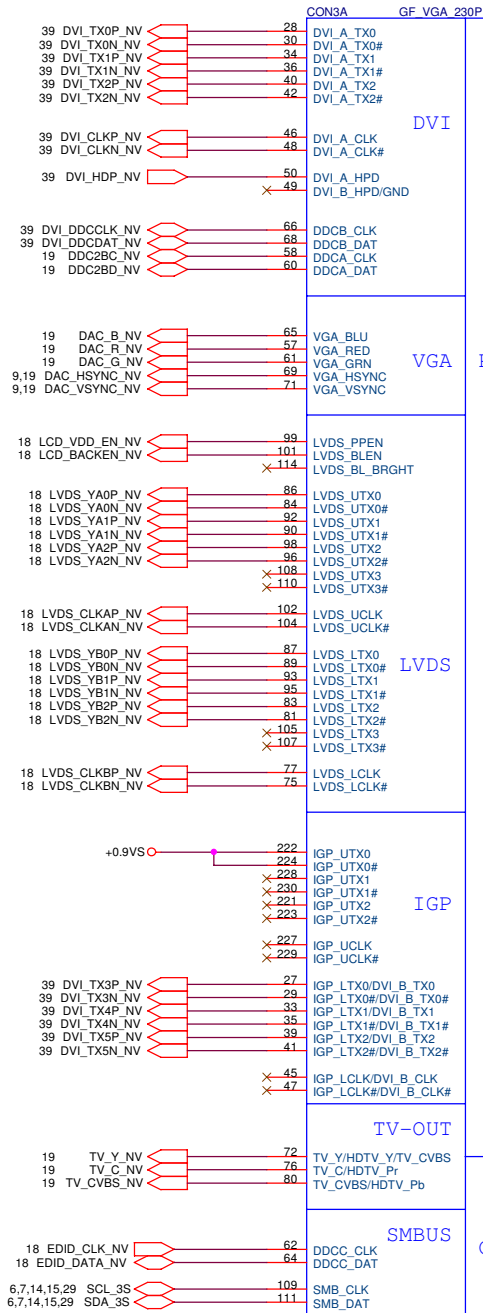




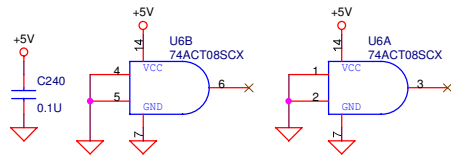
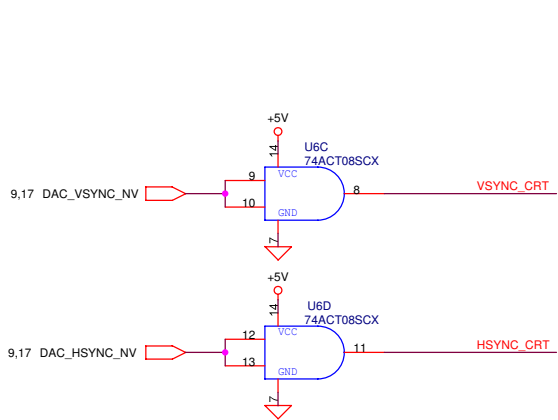
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



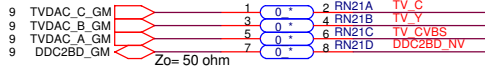
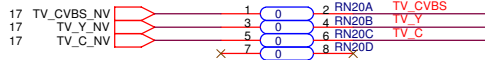
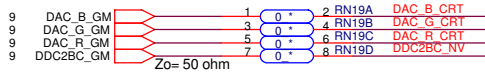
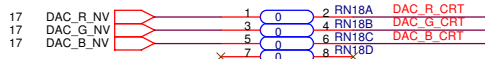
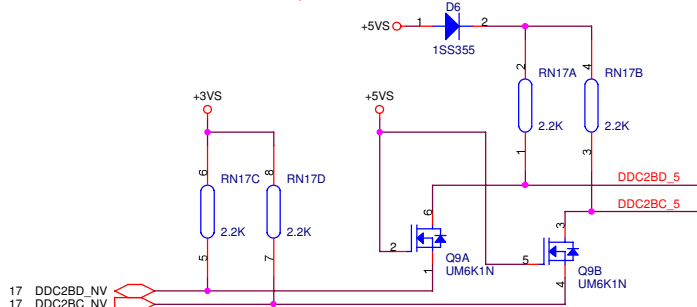
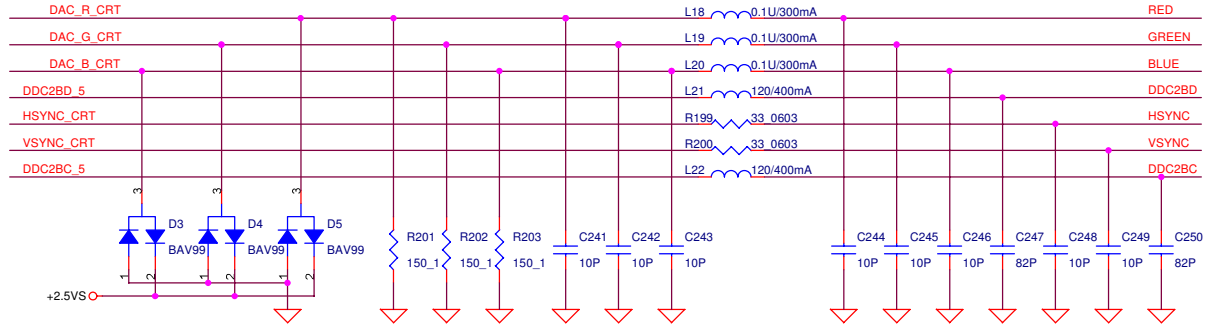
Kennedy_Zhang



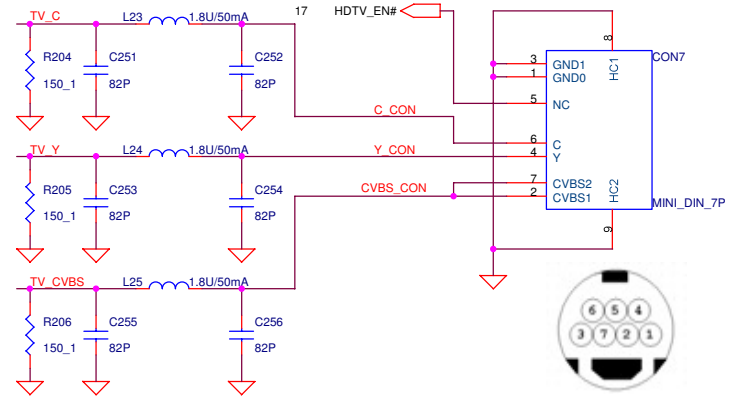
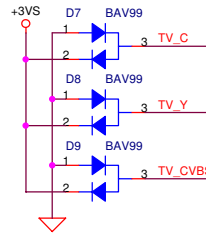
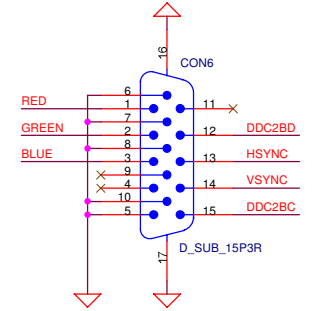
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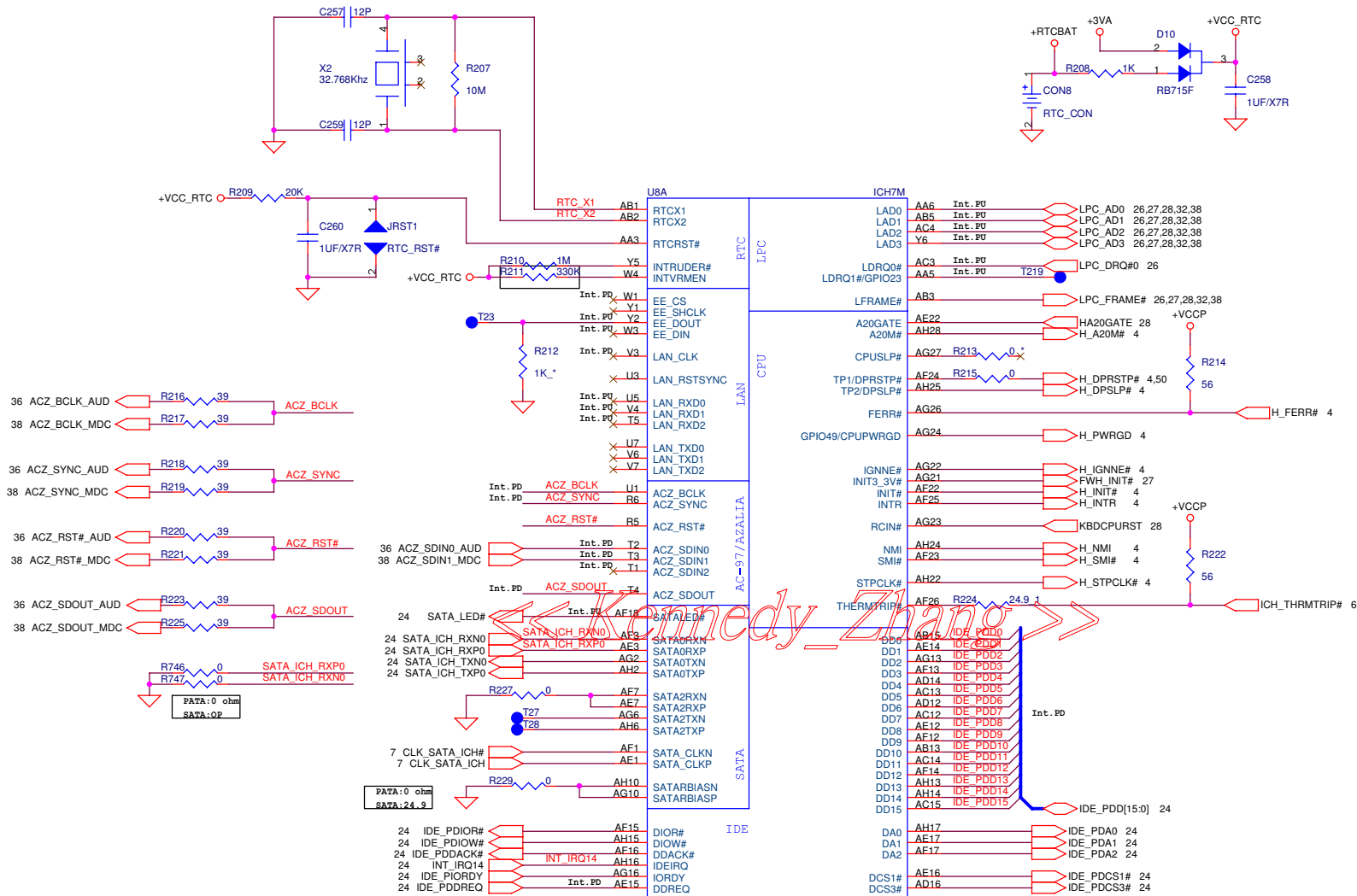


+2.5VS	→	+2.5VS	11,17,38,54
+3VS	→	+3VS	6,7,9,11,13,14,15,17,18,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+5V	→	+5V	15,17,25,28,32,36,38,40,41,59,61
+5VS	→	+5VS	22,23,24,28,29,36,37,38,39,40,41,50,61



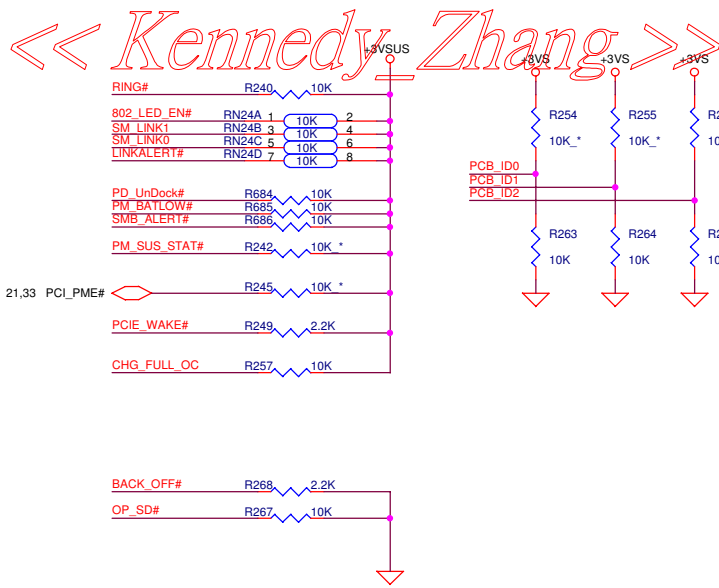
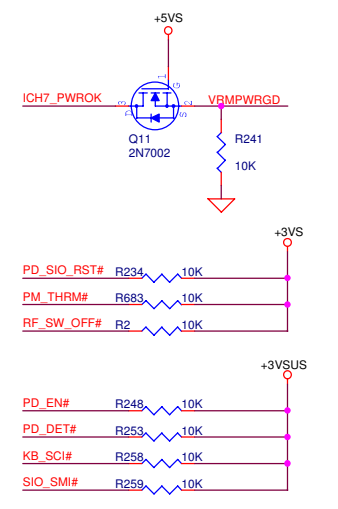
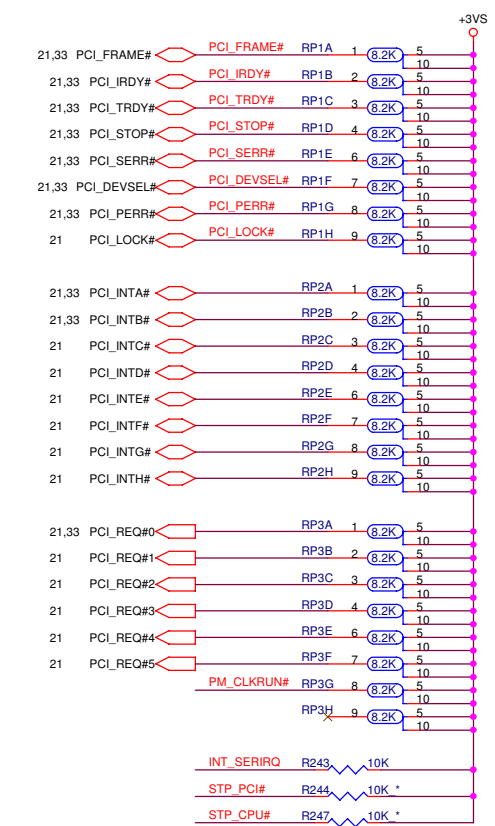
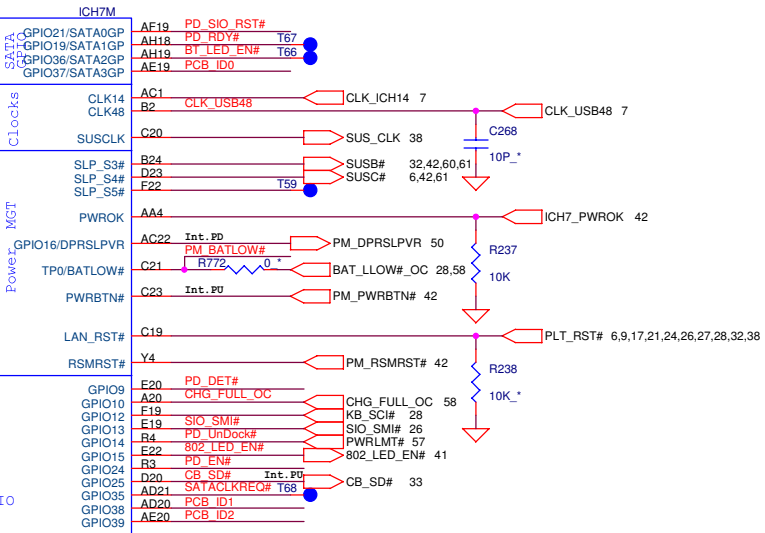
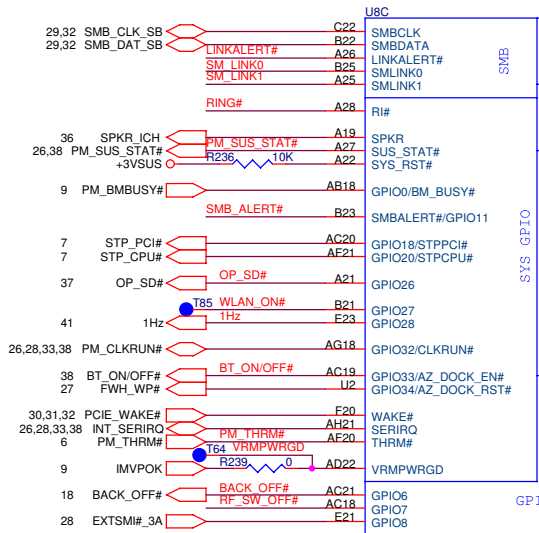
<< Kennedy_Zhang >>



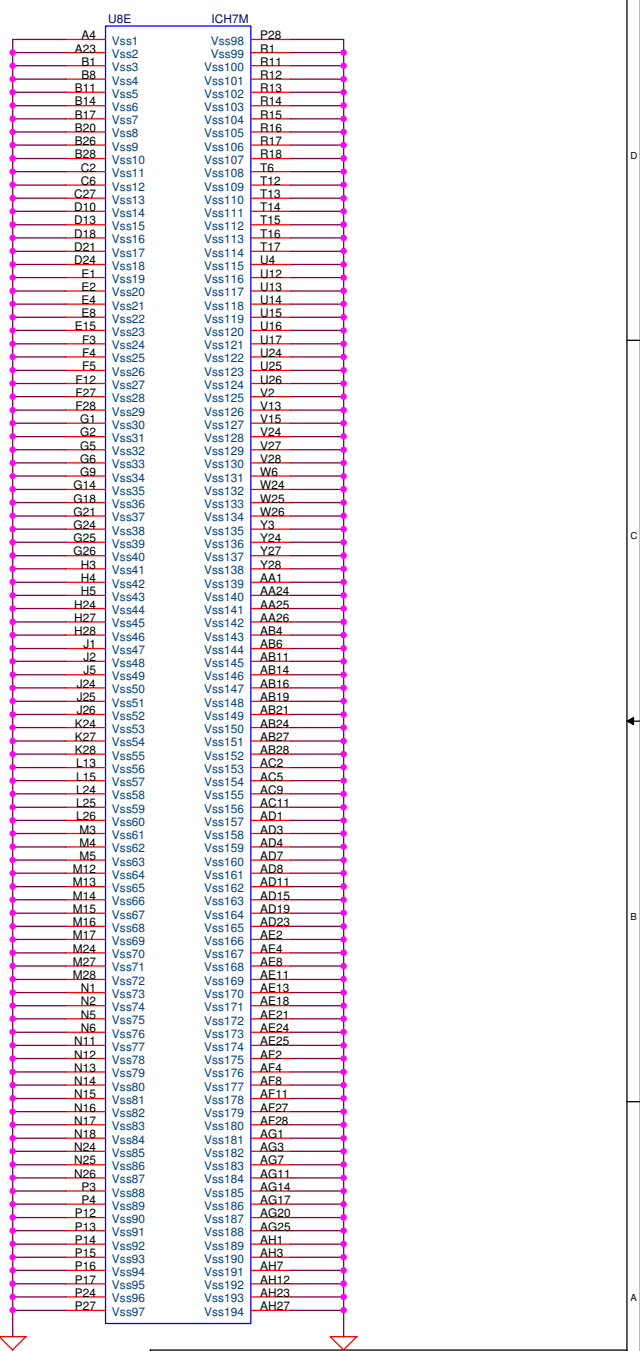
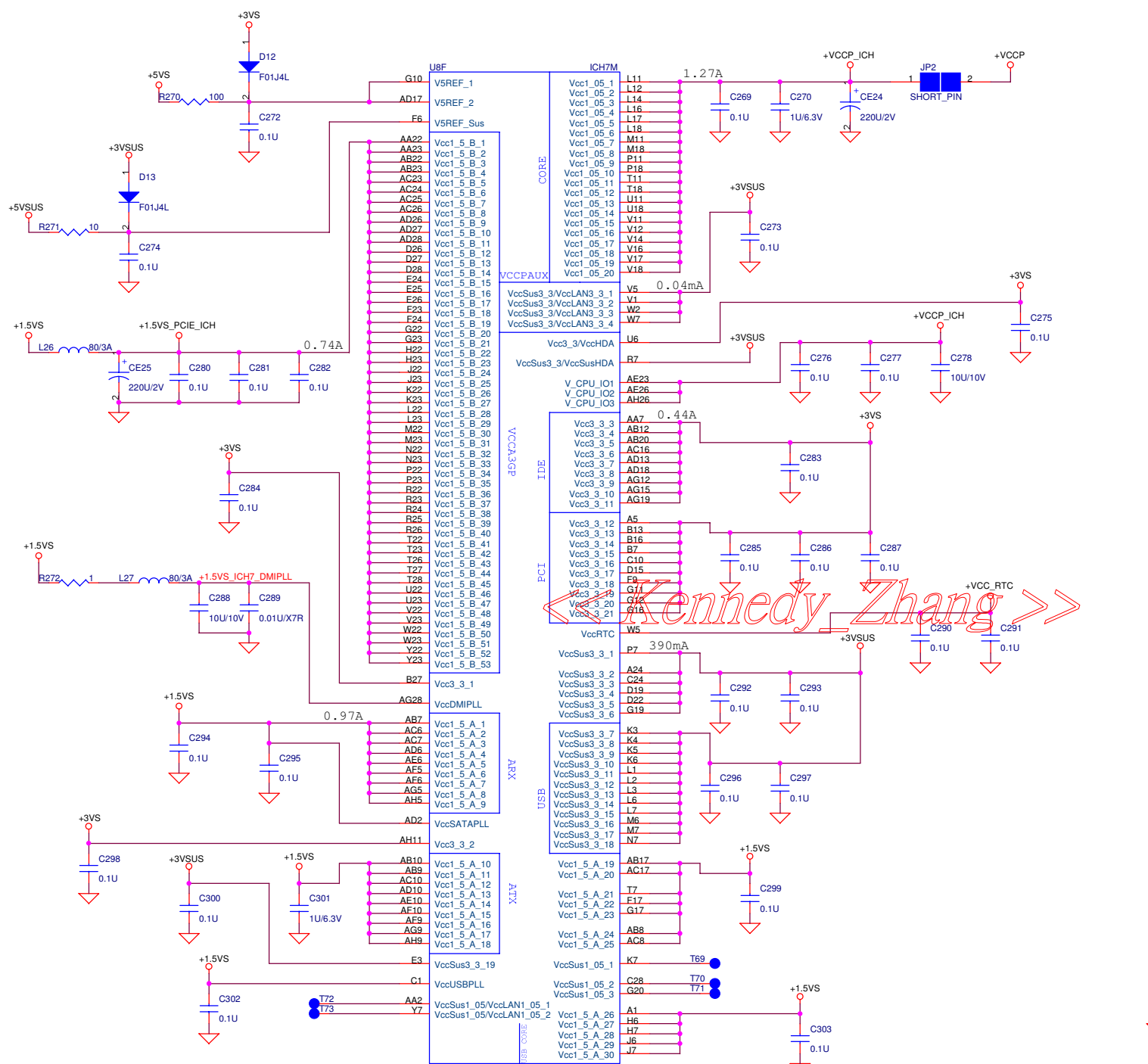


+3VA +3VA 38,41,42,54,59,63
 +VCCP +VCCP 4,5,6,8,11,12,23,52

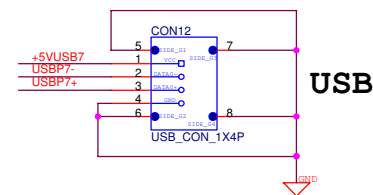
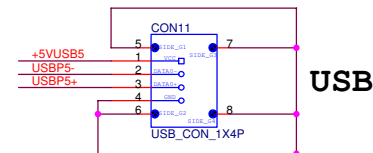
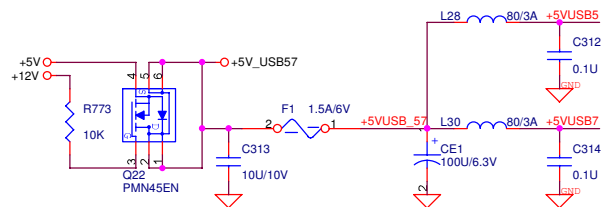
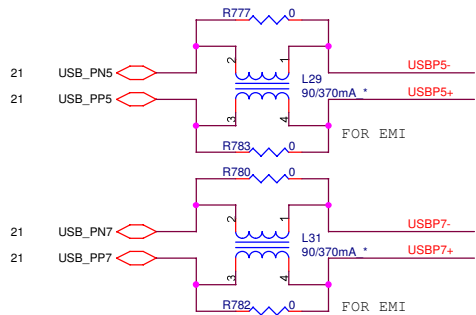
+3VS \rightarrow +3VS 6,7,9,11,13,14,15,17,18,19,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
 +5VS \rightarrow +5VS 19,23,24,28,29,36,37,38,39,40,41,50,61
 +3VSUS \rightarrow +3VSUS 18,21,23,28,29,30,42,51



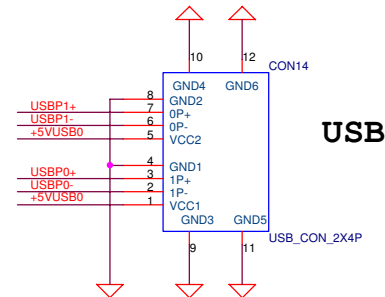
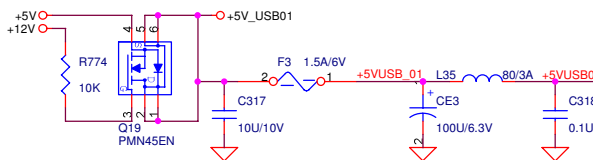
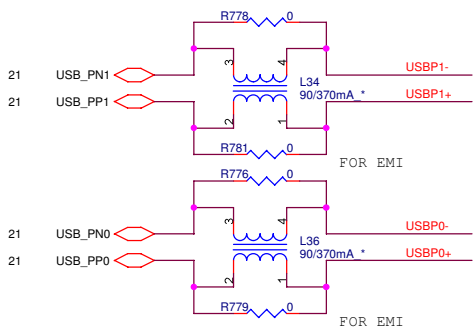
<< Kennedy Zhang >>



+5VSUS	51
+3VSUS	18,21,22,28,29,30,42,51
+5VS	19,22,24,28,29,36,37,38,39,40,41,50,61
+3VS	6,7,9,11,13,14,15,17,18,19,22,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+1.5VS	5,9,11,12,17,31,32,38,52
+VCCP	4,5,6,8,11,12,20,52

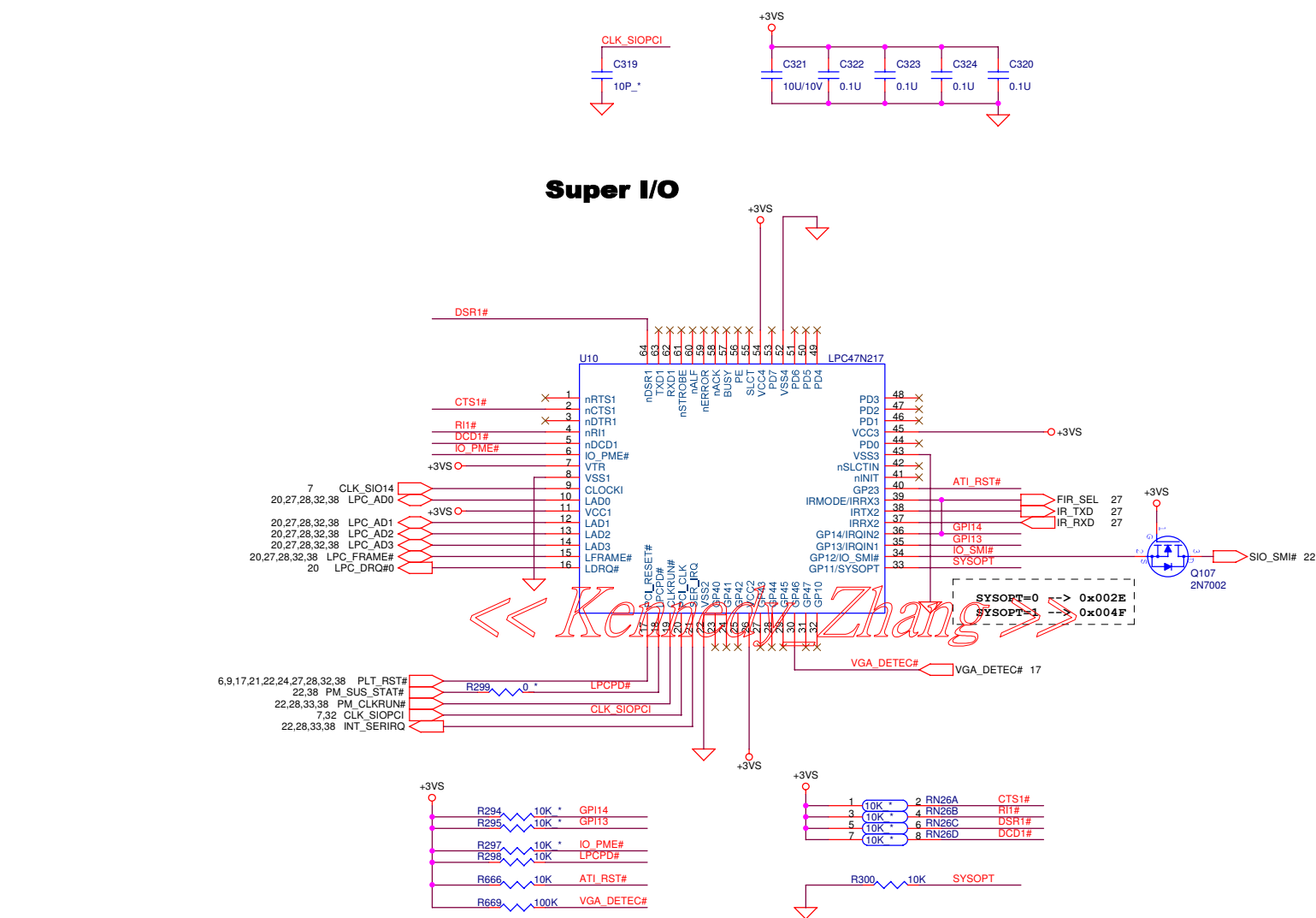


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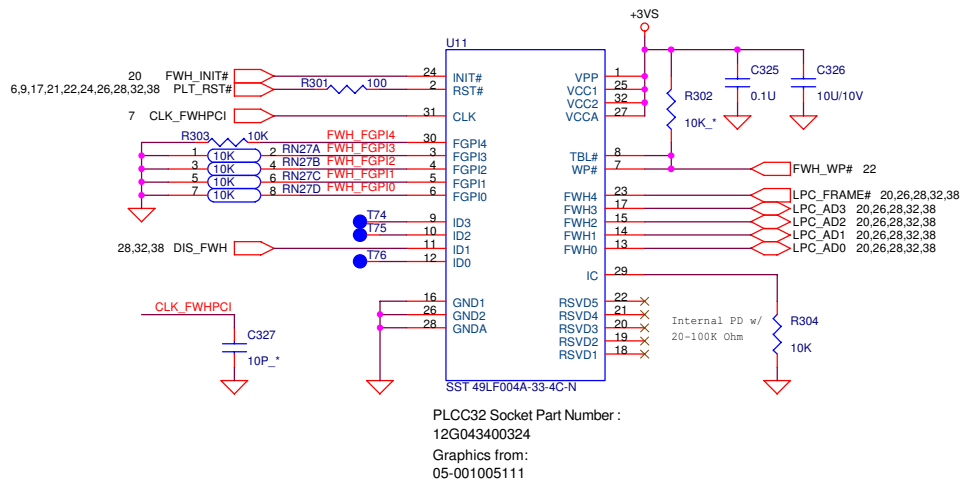
+5V +5V 15,17,19,28,32,36,38,40,41,59,61

Super I/O

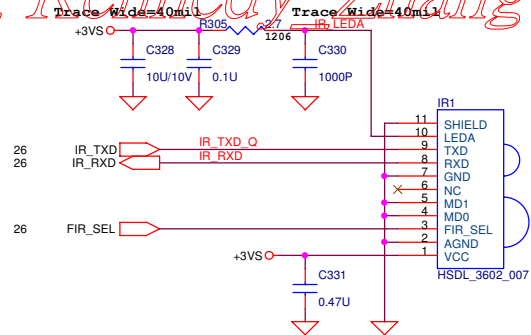


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+3VS +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61



<< Kennedy Zhang >>

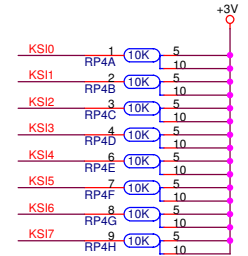
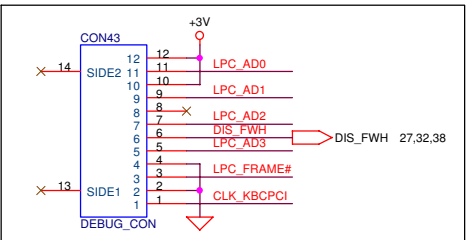


+3VS +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61

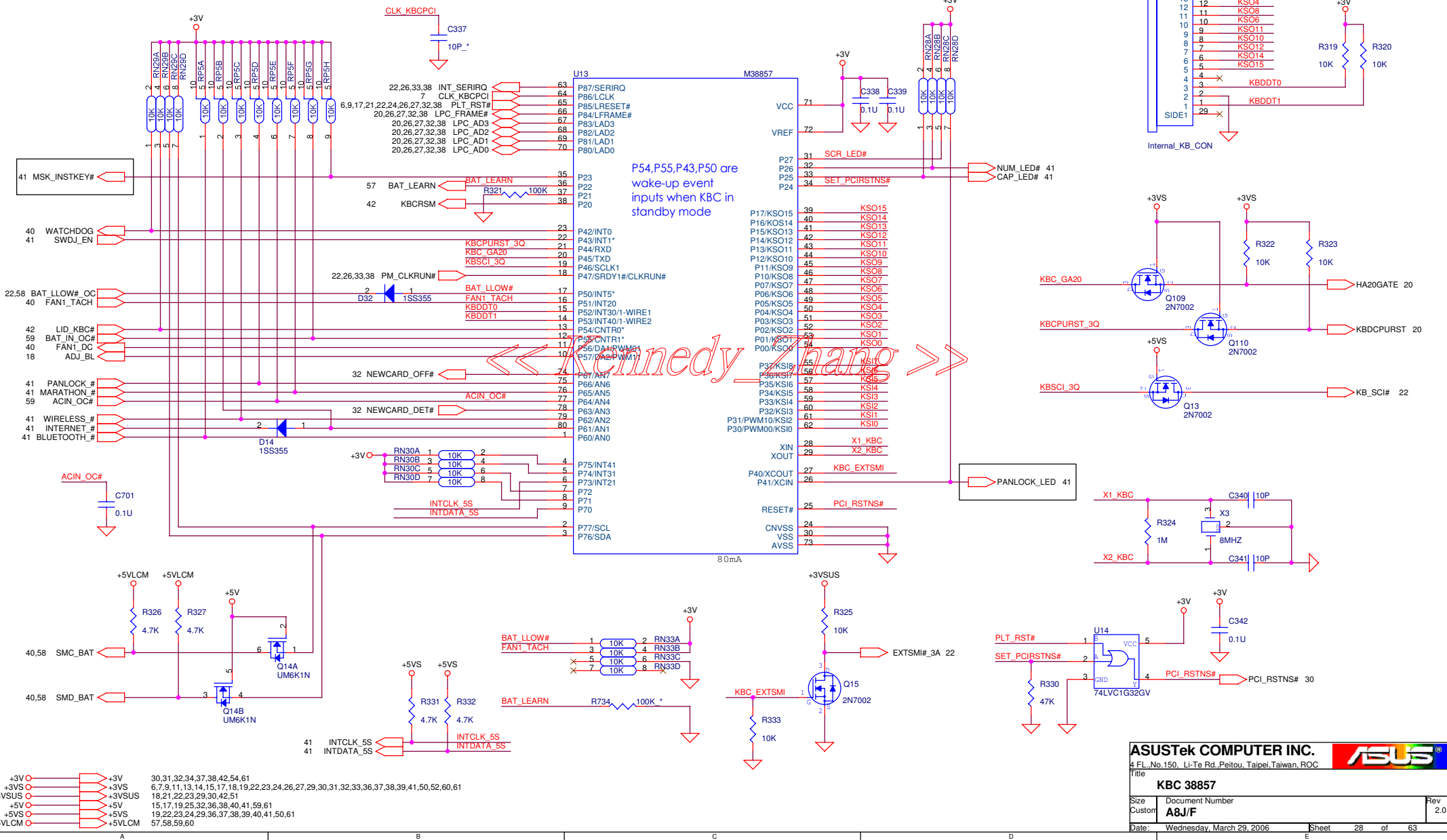
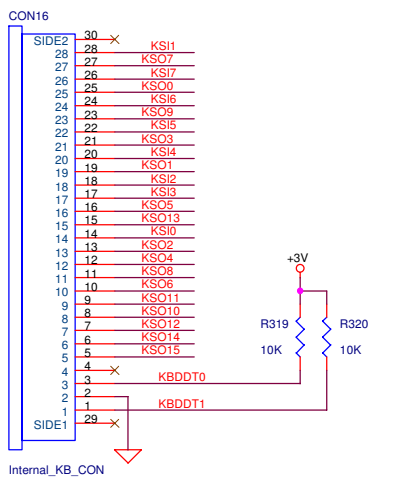
P2.1 Low : Power Button Override disable
Input Event only at P54, P55, P43, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.



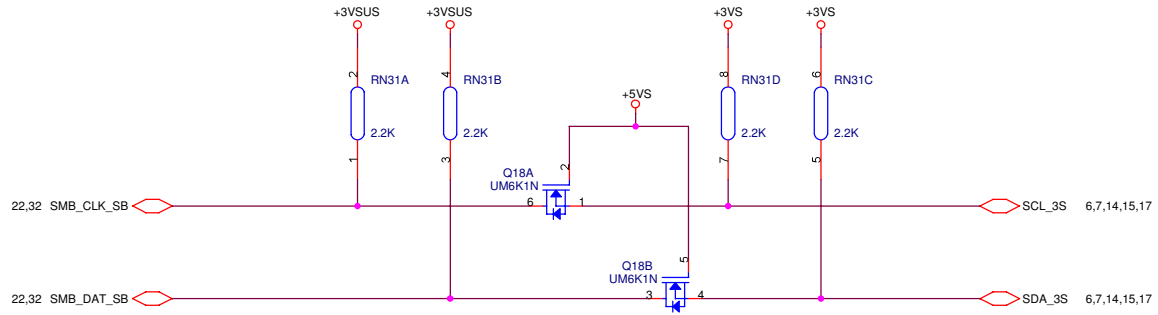
KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP



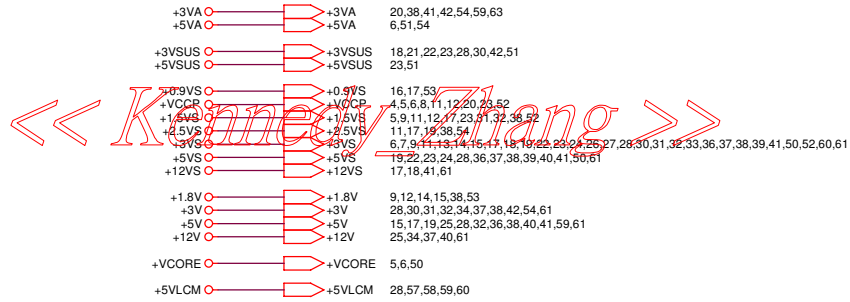
P54, P55, P43, P50 are wake-up event inputs when KBC in standby mode

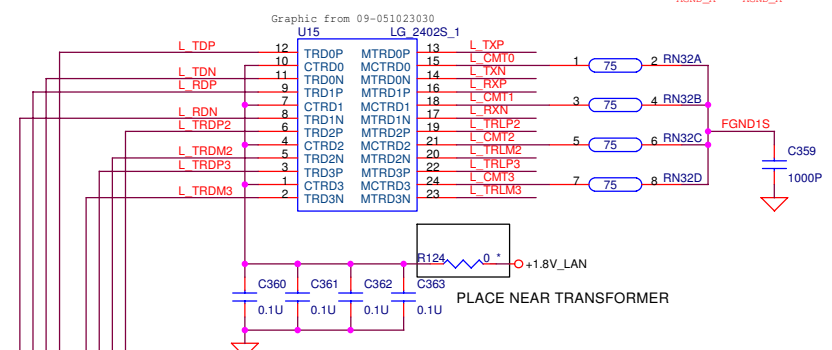
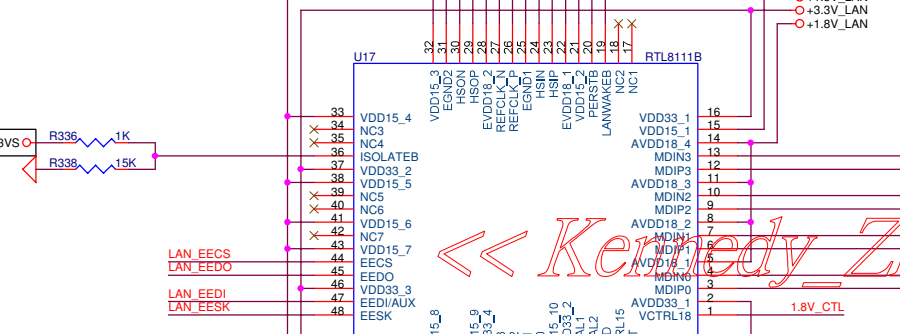
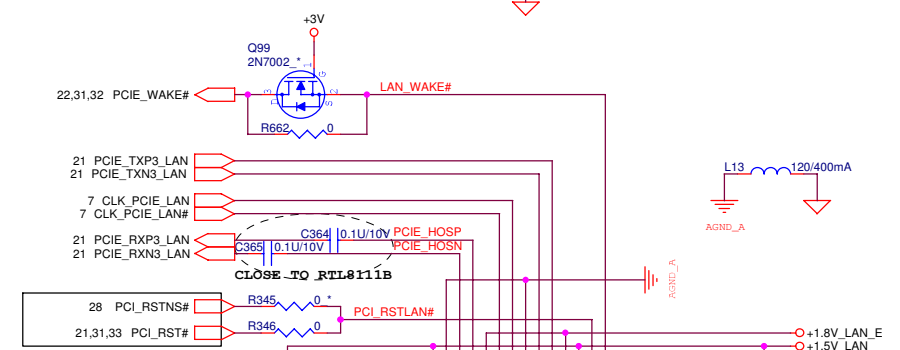
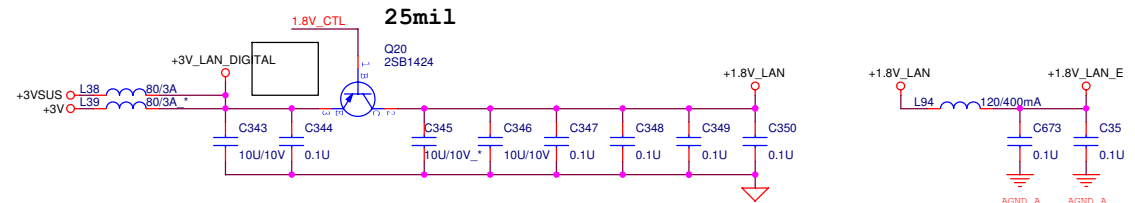
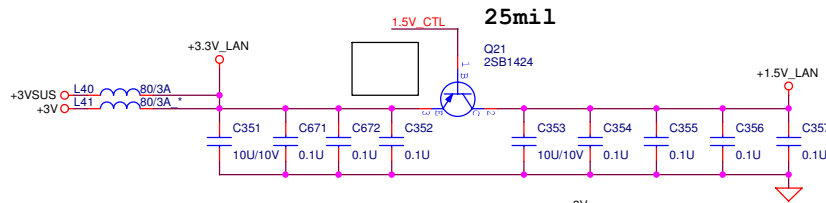
Kennedy Zhang

ICH7-M

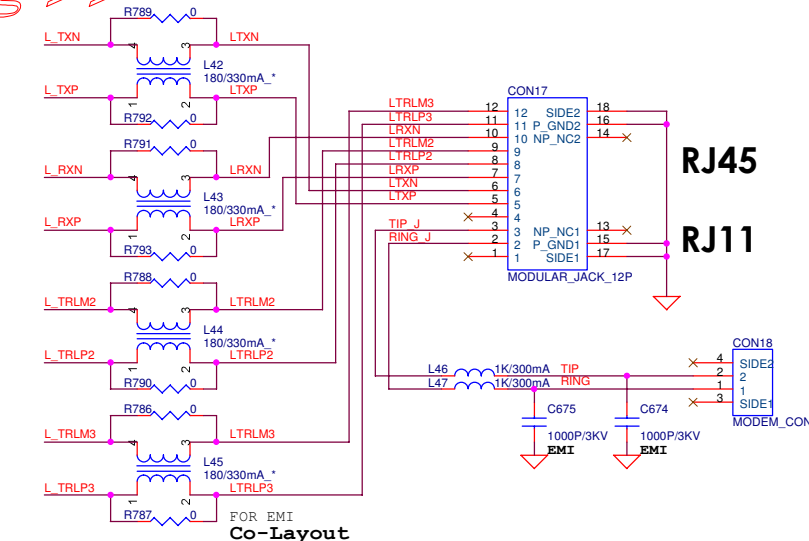
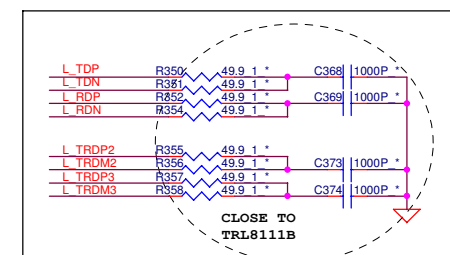
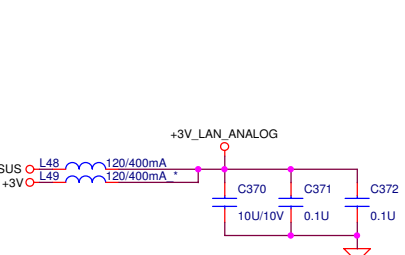
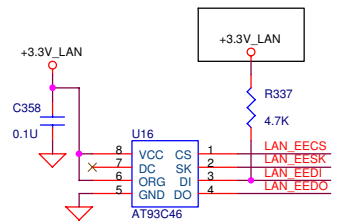


Termal Sensor,
Clock Generator
DDR2 SO-DIMM
TPM



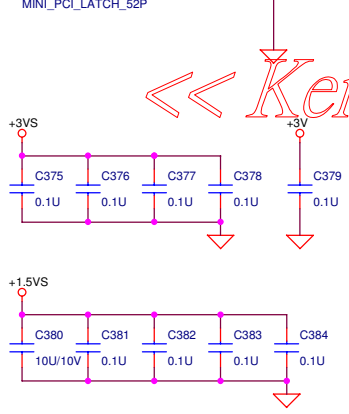
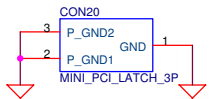
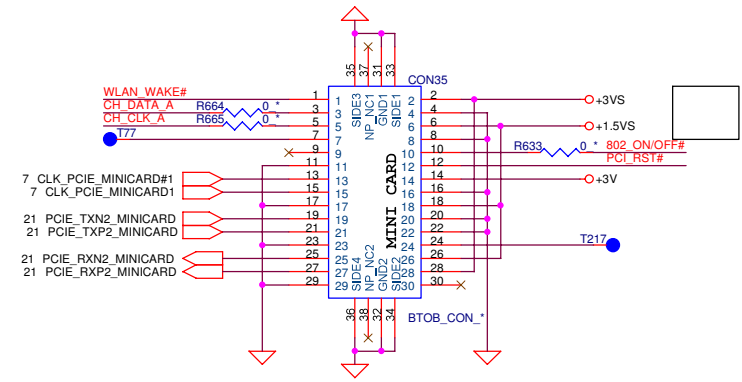
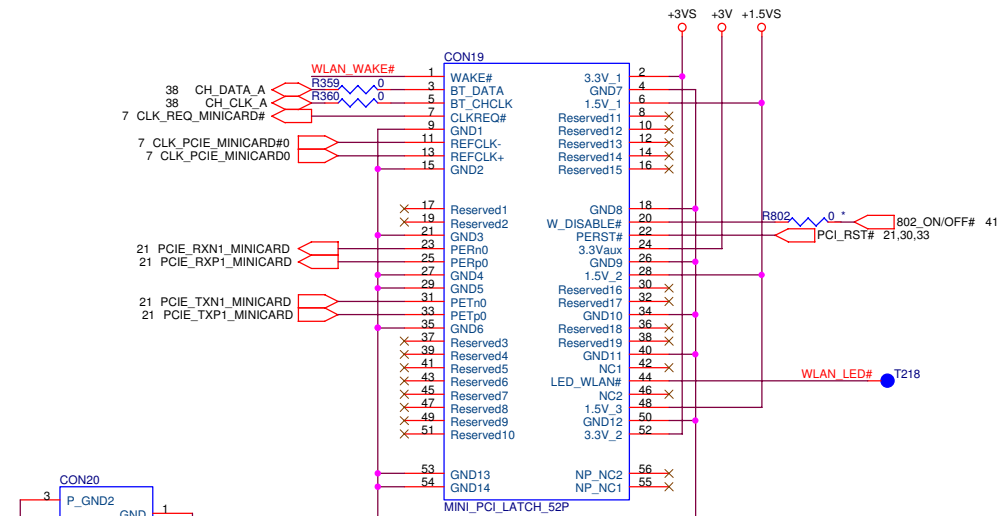


<< Kennedy_Zhang >>



FOR EMI
Co-Layout

+3V	28,31,32,34,37,38,42,54,61
+3VSUS	18,21,22,23,28,29,42,51



<< Kennedy_Zhang >>

+1.5VS	5, 9, 11, 12, 17, 23, 32, 38, 52
+3V	28, 30, 32, 34, 37, 38, 42, 54, 61
+3VS	6, 7, 9, 11, 13, 14, 15, 17, 18, 19, 22, 23, 24, 26, 27, 28, 29, 30, 32, 33, 36, 37, 38, 39, 41, 50, 52, 60, 61

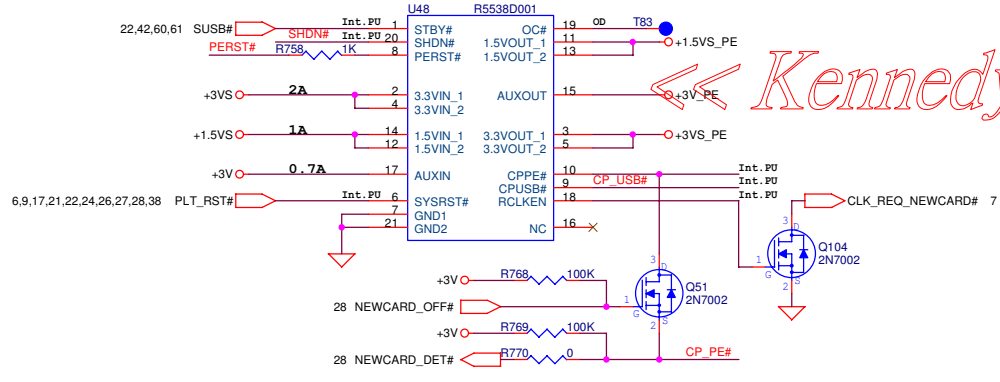
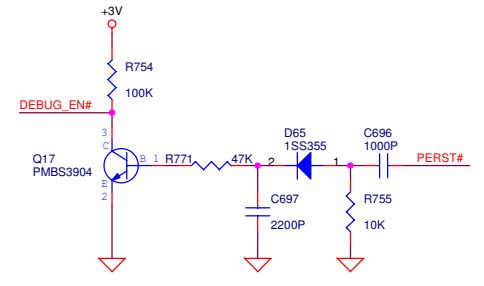
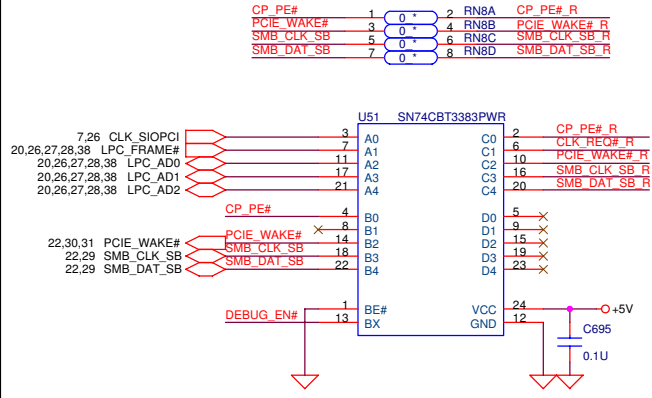
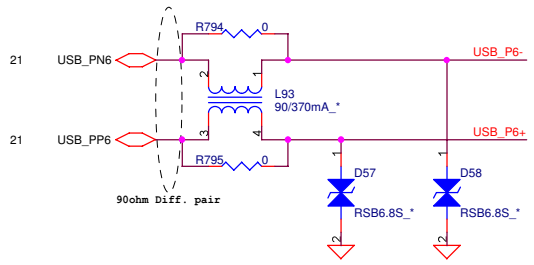
ASUSTek COMPUTER INC.

4 FL, No. 150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

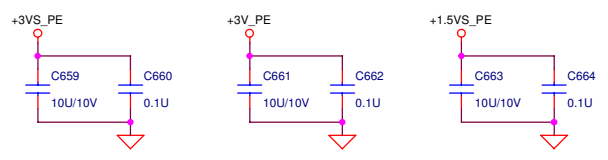
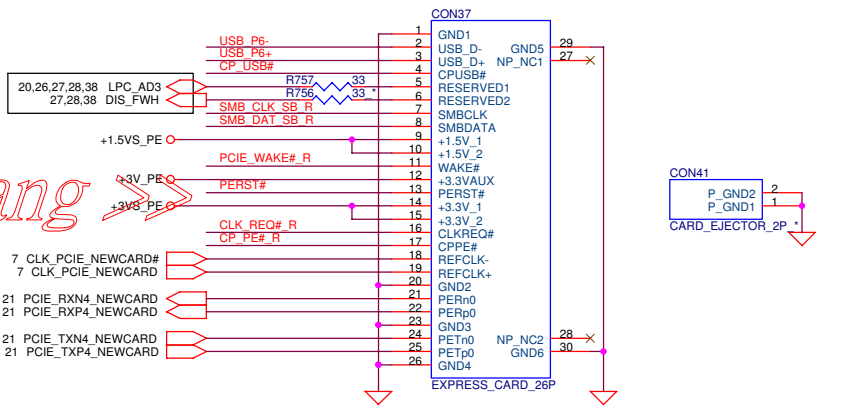
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Size	Document Number	Rev
Custom	A8J/F	2.0

Date: Wednesday, March 29, 2006 Sheet 31 of 63

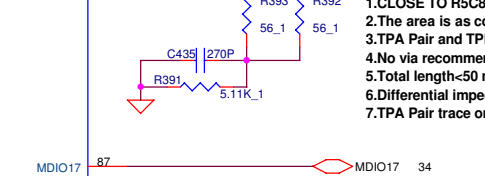
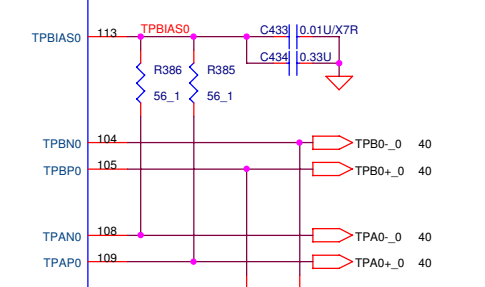
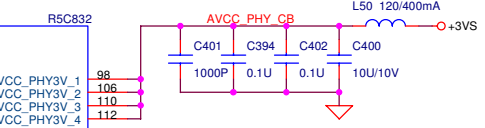
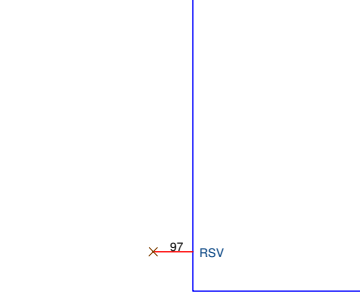
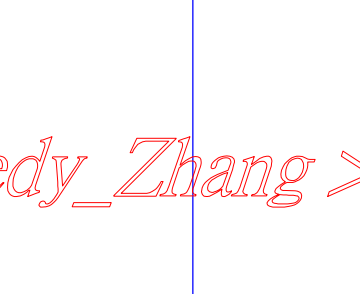
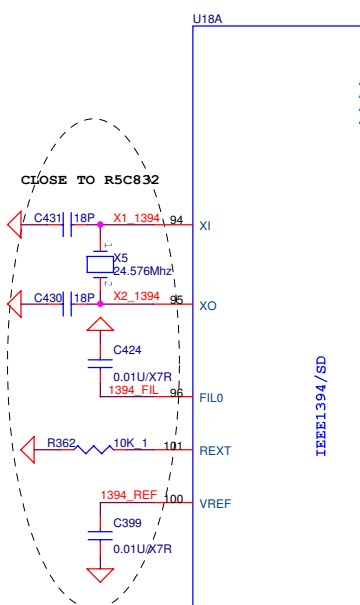
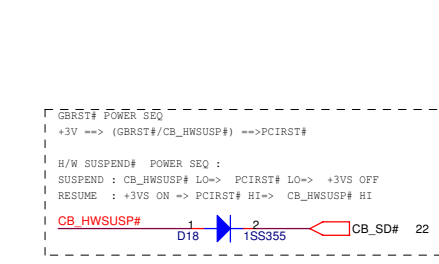
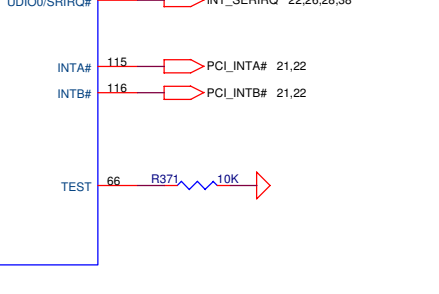
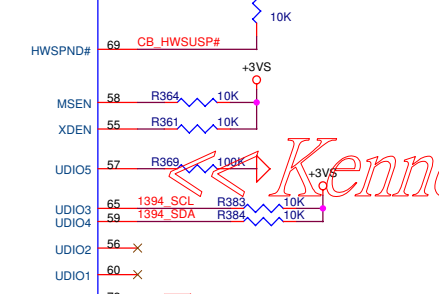
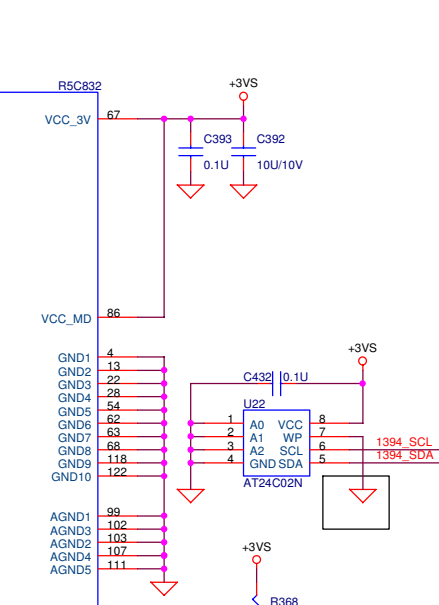
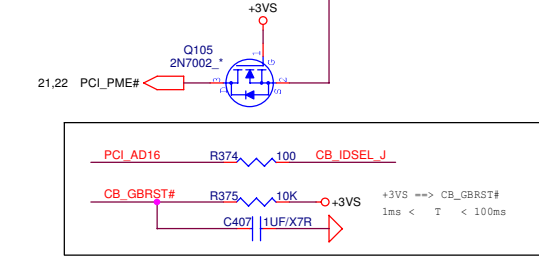
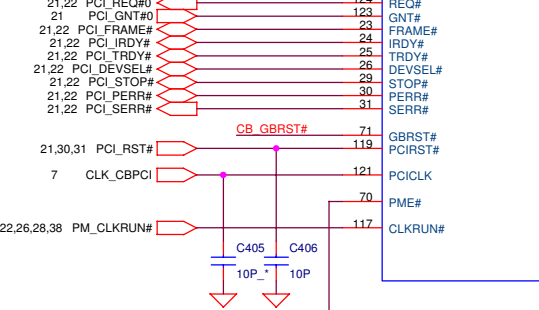
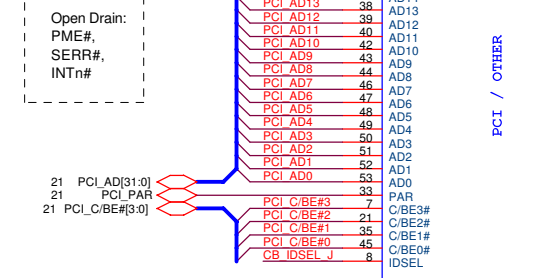
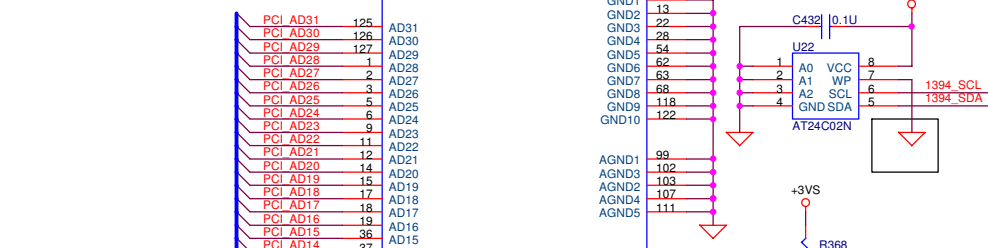
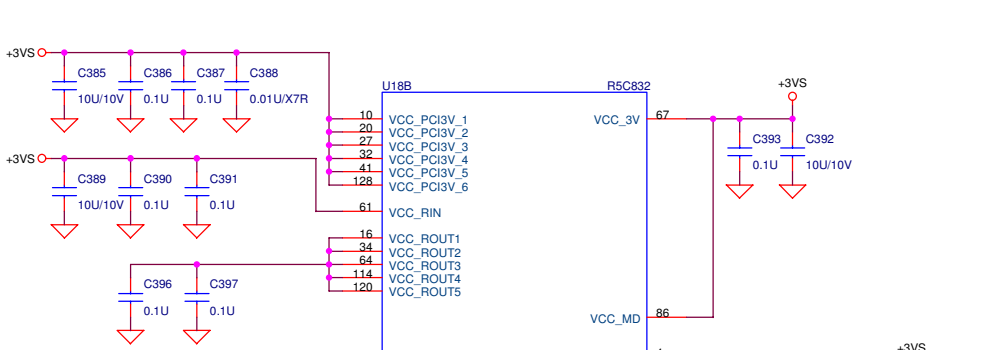


Kennedy_Zhang



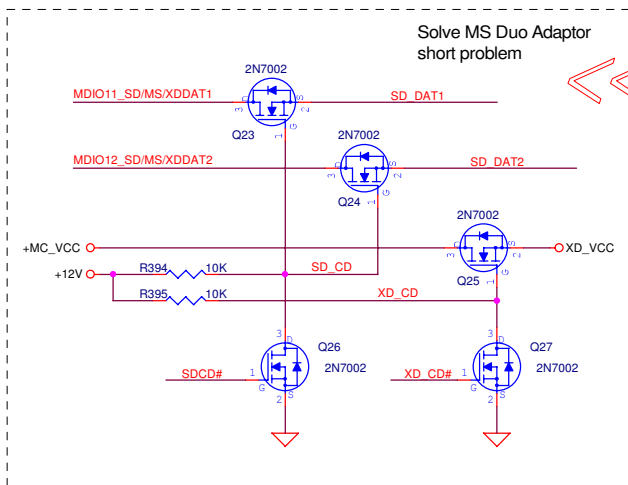
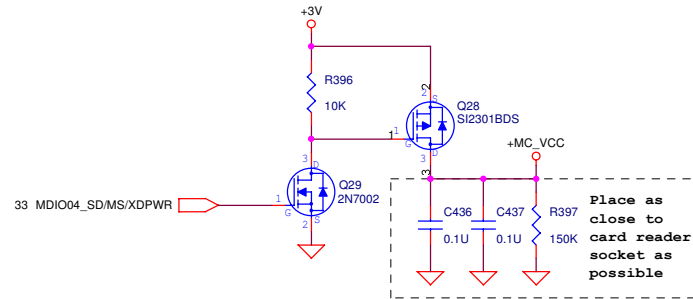
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- +3VS → +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,33,36,37,38,39,41,50,52,60,61
- +3V → +3V 28,30,31,34,37,38,42,54,61

+3VS 6,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,36,37,38,39,41,50,52,60,61

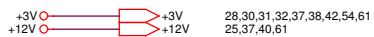
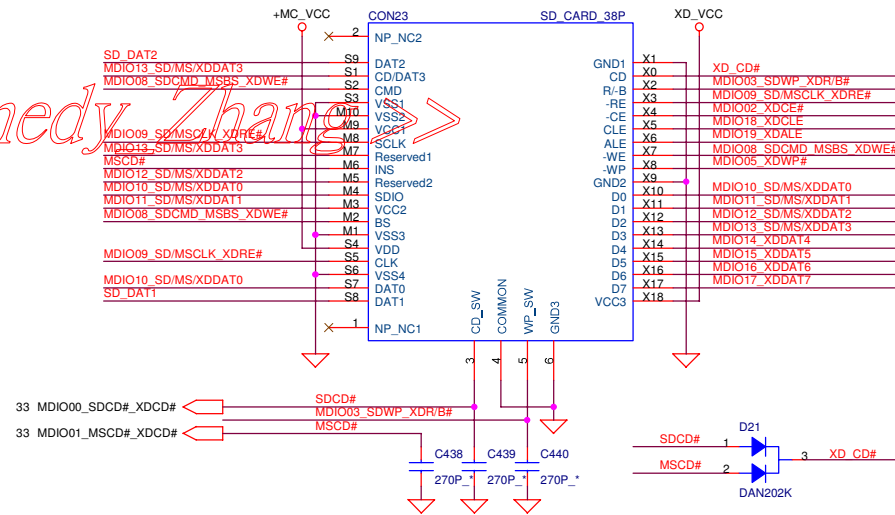


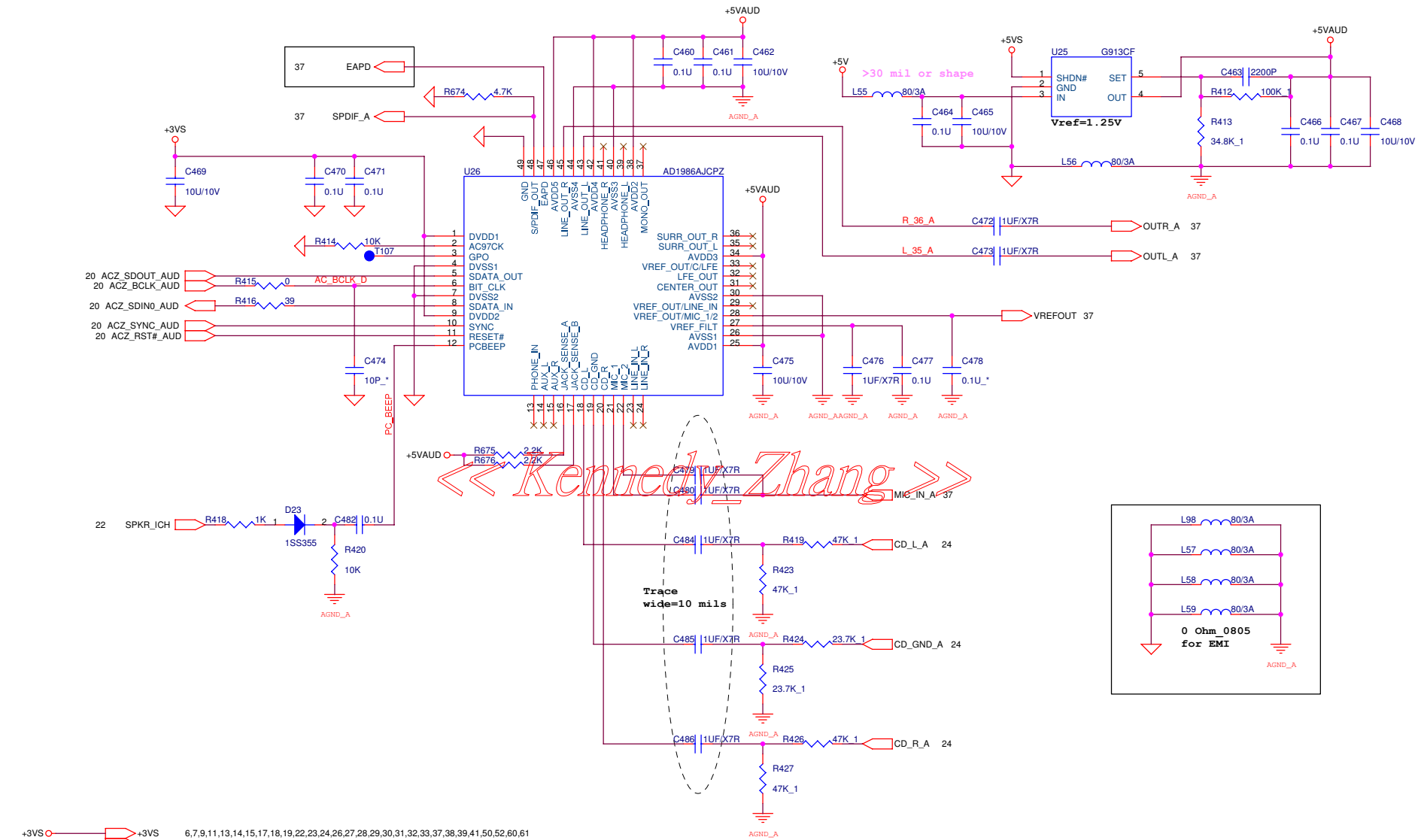
1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10mm
3. TPA pair and TPB pair mismatch < 2.5mm
4. No via recommend, maximum is one.
5. Total length < 50mm
6. Differential impedance is 110 +/- 6 ohm
7. TPA pair trace or TPB pair trace mismatch < 1.25mm

MDIO0-> SD Card Detect
 MDIO1-> MS Card Detect
 MDIO3-> SD Write Protect /XD Card Ready/Busy#
 MDIO4-> SD/MS/XD Card Power Control
 MDIO5-> XD Card Write Protect
 MDIO6-> SD/MS/SD LED
 MDIO7-> SD/MS External Clock
 MDIO8-> SD Command/MS Bus State /XD Card Write Enable
 MDIO9-> SD/MS Clock /XD Card Read Enable
 MDIO10-> SD/MS/XD Data 0
 MDIO11-> SD/MS/XD Data 1
 MDIO12-> SD/MS/XD Data 2
 MDIO13-> SD/MS/XD Data 3
 MDIO14-> XD Data 4
 MDIO15-> XD Data 5
 MDIO16-> XD Data 6
 MDIO17-> XD Data 7
 MDIO18-> XD Command Latch
 MDIO19-> XD Card Address Latch

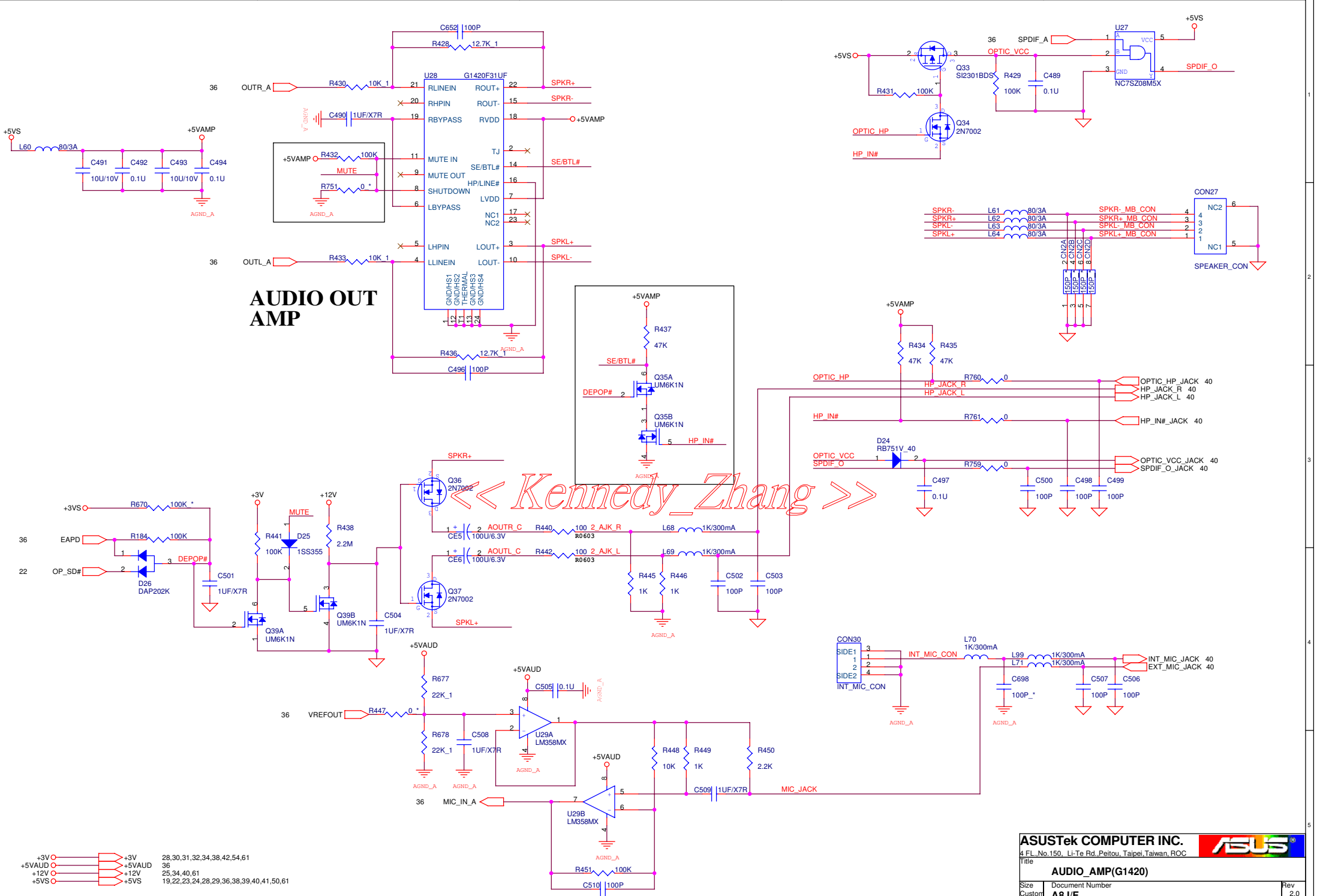


« Kennedy Zhang »





+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,37,38,39,41,50,52,60,61
+5V	15,17,19,25,28,32,38,40,41,59,61
+5VS	19,22,23,24,28,29,37,38,39,40,41,50,61
+5VAUD	37



AUDIO OUT AMP

<< Kennedy_Zhang >>

+3V	28,30,31,32,34,38,42,54,61
+5VAUD	36
+12V	25,34,40,61
+5VS	19,22,23,24,28,29,36,38,39,40,41,50,61

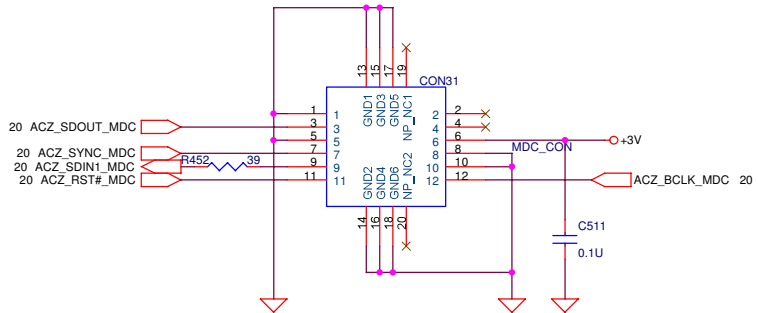
ASUSTek COMPUTER INC.

4 FL, No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

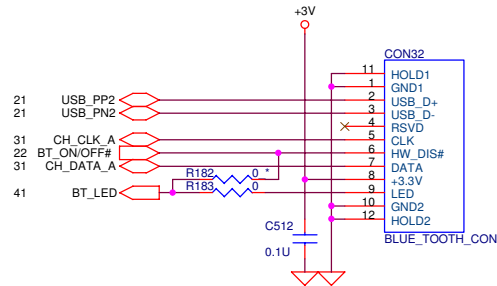
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Size	Document Number	Rev
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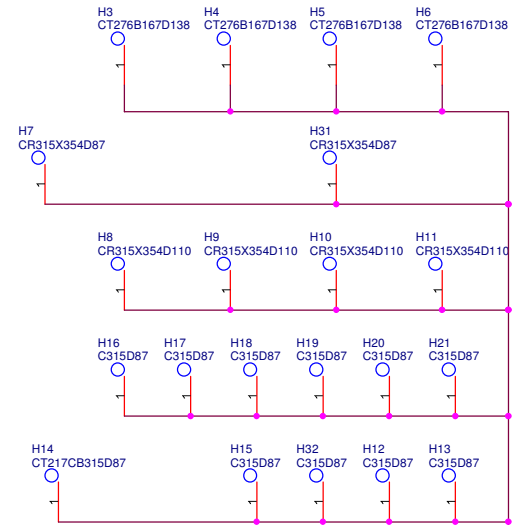
Date: Wednesday, March 29, 2006 Sheet 37 of 63



Azalia MDC MODEM CON



Bluetooth Module CON

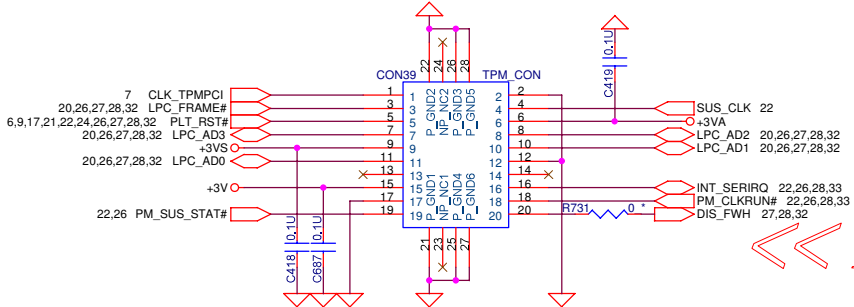


CPU

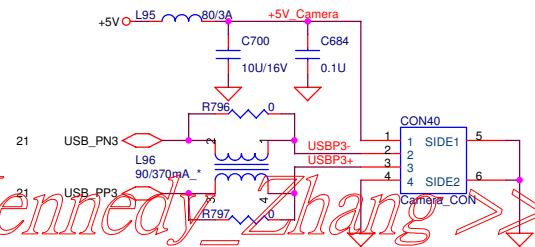
SCREW

U HOLE

SCREW

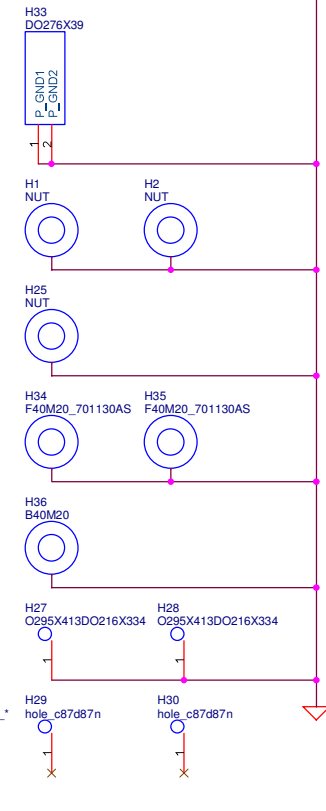


TPM Module CON



Camera Module CON

<< Kennedy_Zhang >>



IO Board

MDC_NUT

TPM_NUT

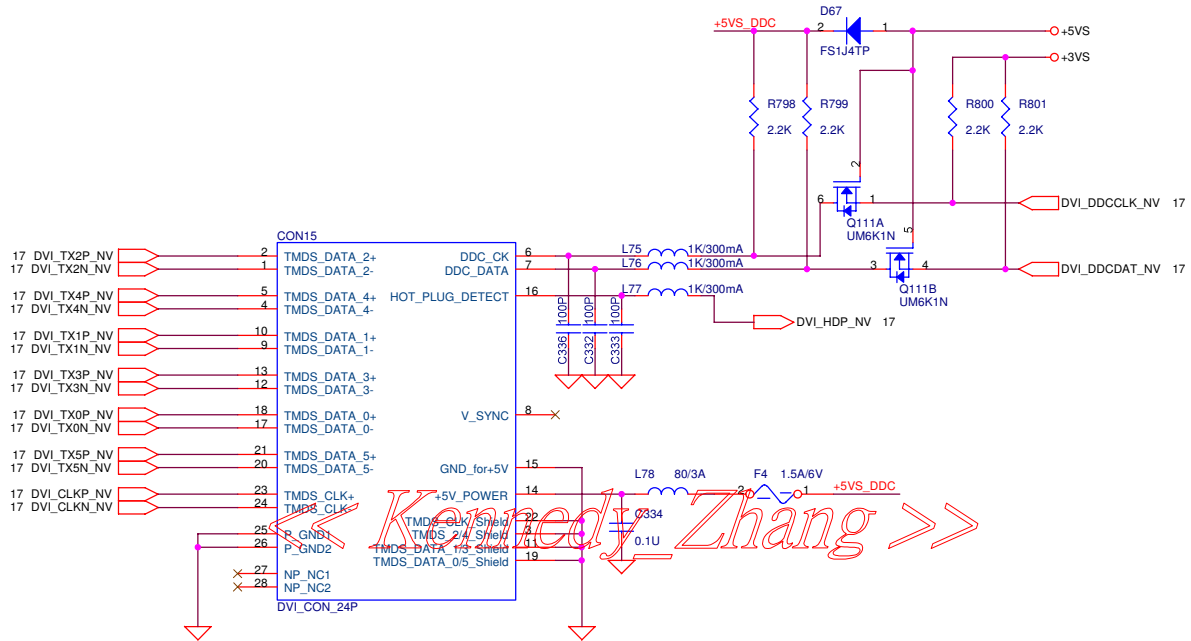
VGA_NUT

KB_NUT

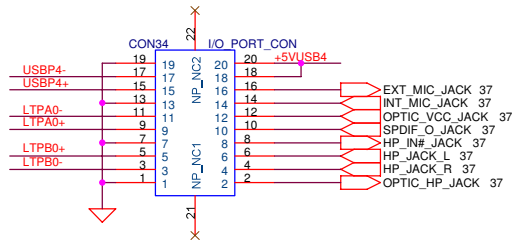
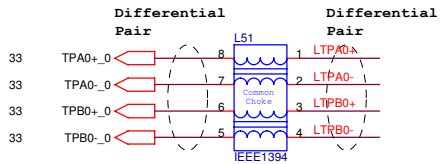
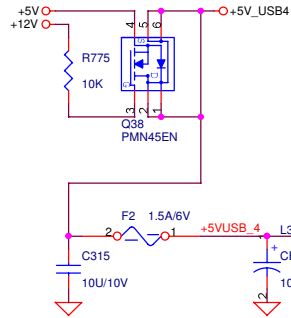
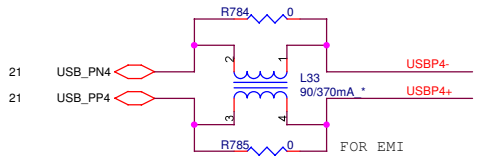
KEYBOARD

FIXED HOLE

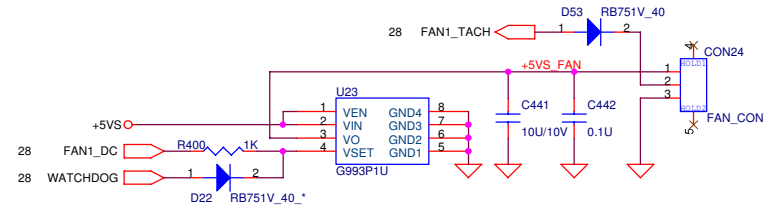
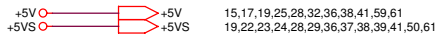
+1.5VS	5,9,11,12,17,23,31,32,52
+1.8V	9,12,14,15,53
+2.5VS	11,17,19,54
+3V	28,30,31,32,34,37,42,54,61
+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,39,41,50,52,60,61
+5V	15,17,19,25,28,32,36,40,41,59,61
+5VS	19,22,23,24,28,29,36,37,39,40,41,50,61



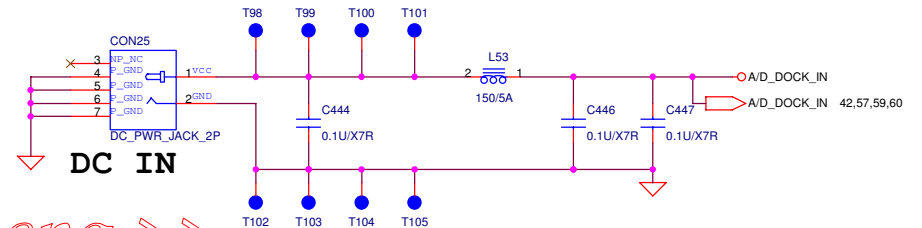
+5VS +5VS 19,22,23,24,28,29,36,37,38,40,41,50,61



I/O PORT

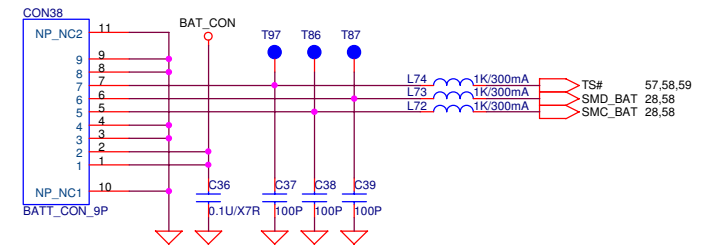


FAN CONTROL



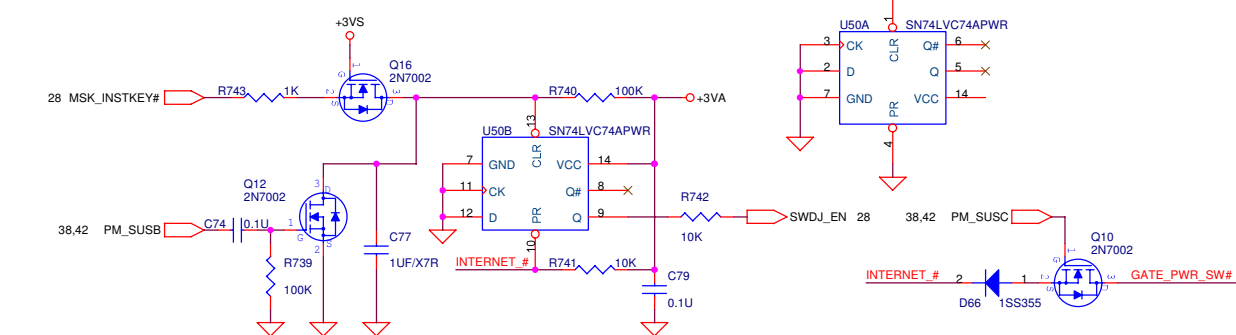
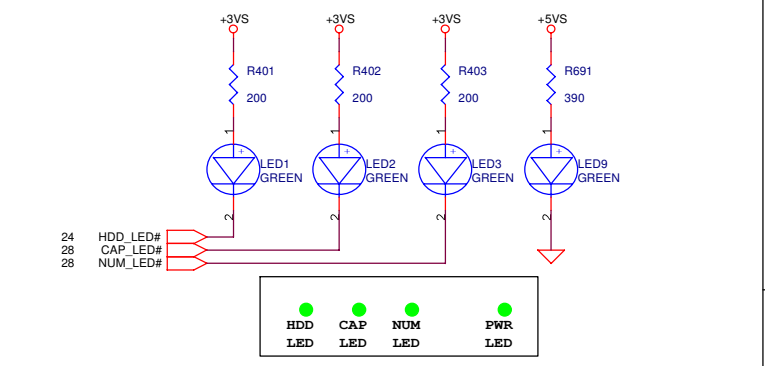
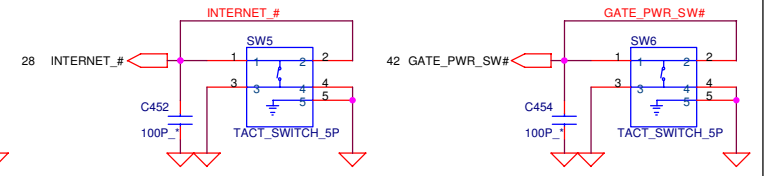
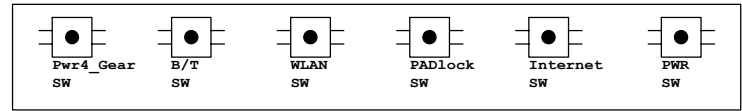
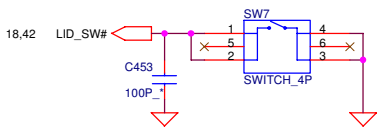
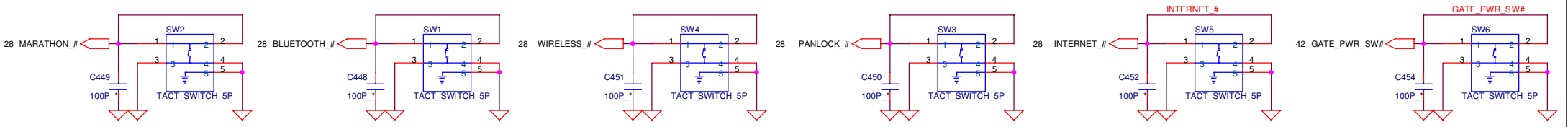
DC IN

ACIN_CONN

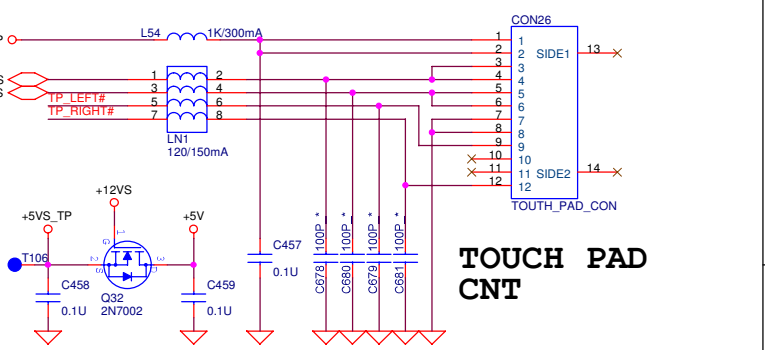
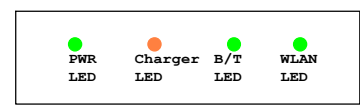
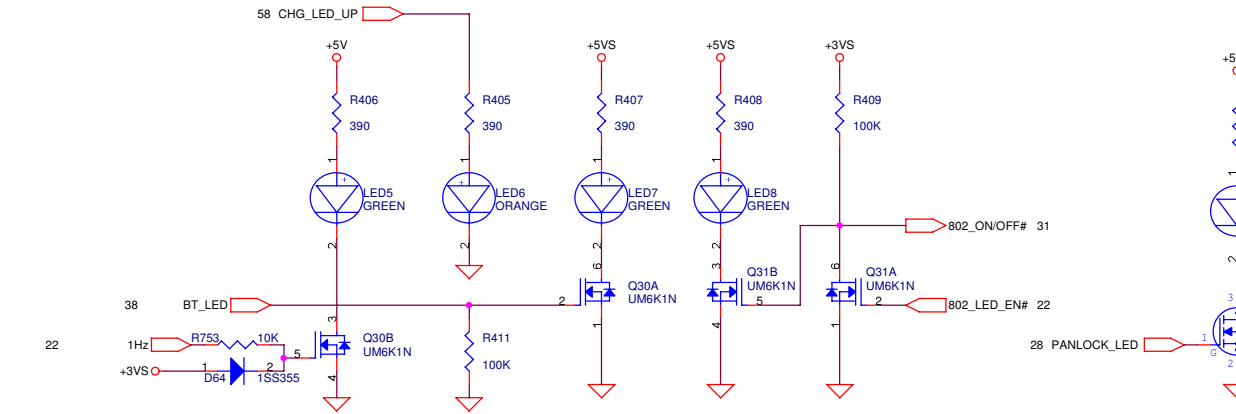
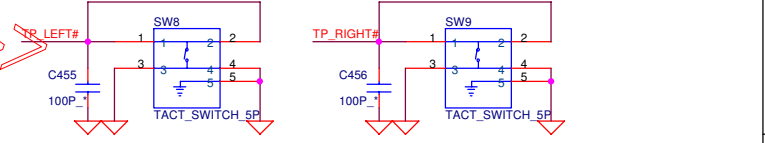


BAT_CONN

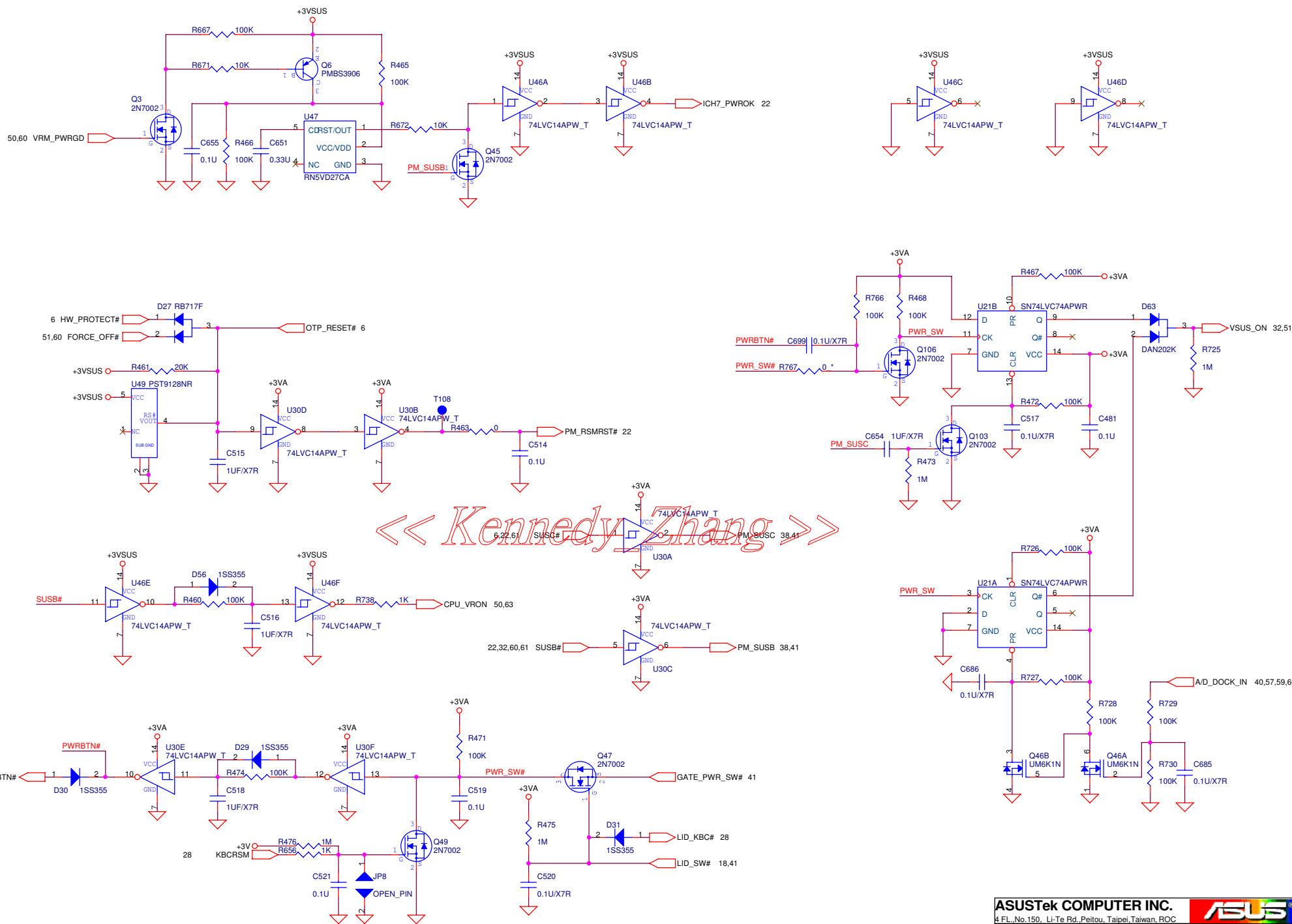
<< Kennedy_Zhang >>



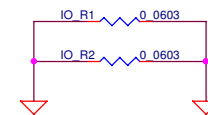
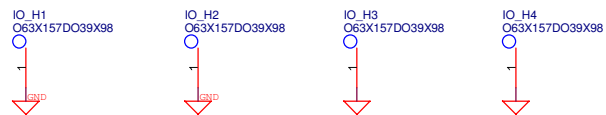
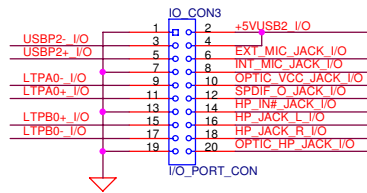
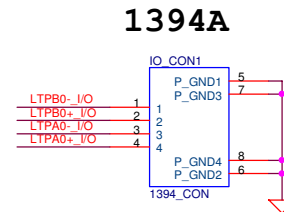
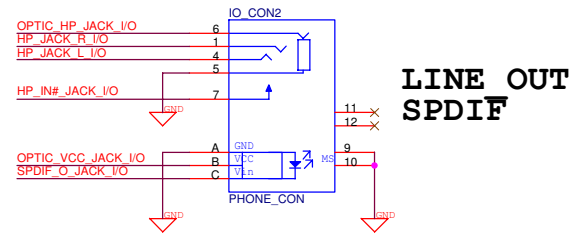
<< Kennedy_Zhang >>

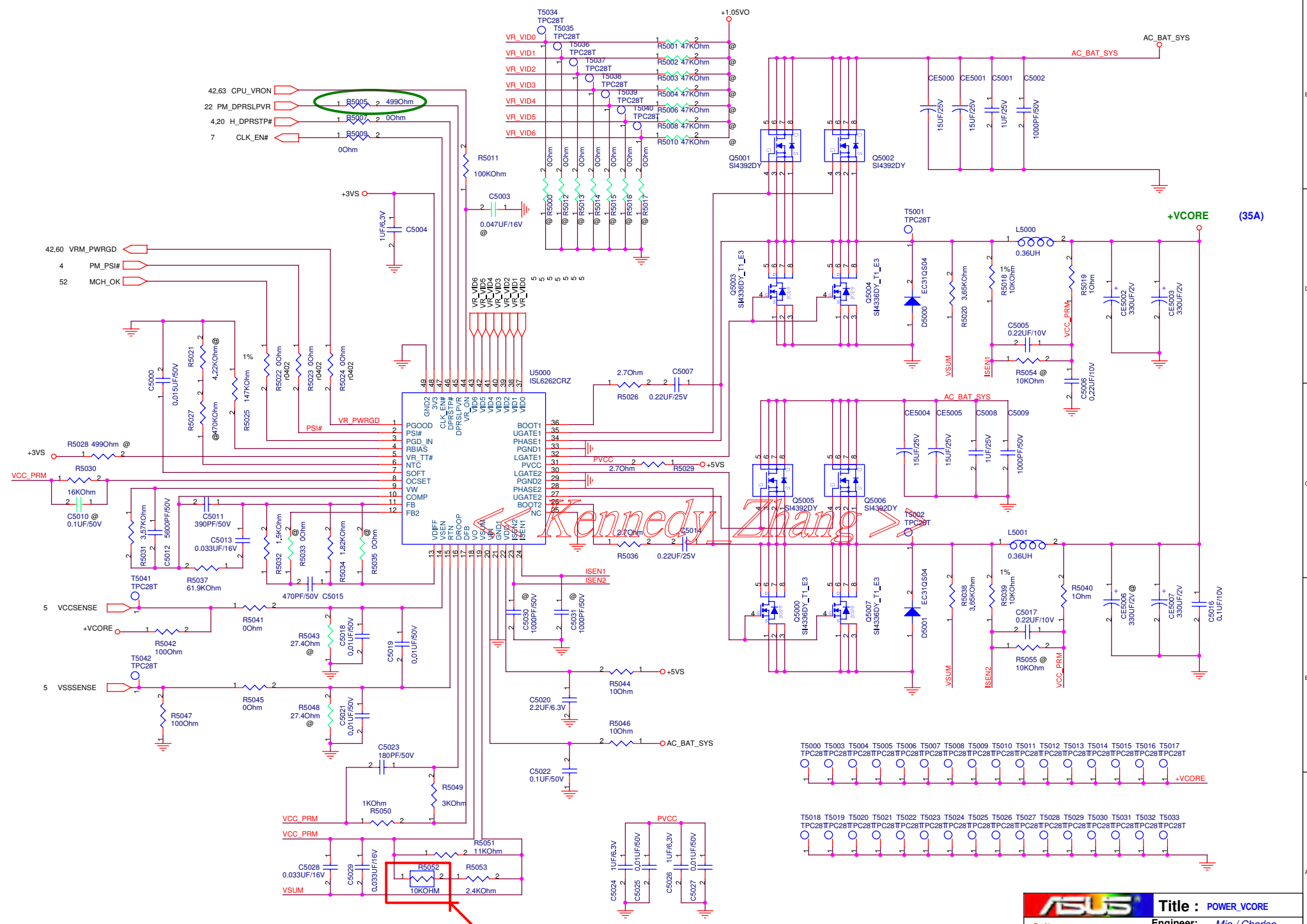


+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,50,52,60,61
+5V	15,17,19,25,28,32,36,38,40,59,61
+5VS	19,22,23,24,28,29,36,37,38,39,40,50,61
+12VS	17,18,61



+3V 28,30,31,32,34,37,38,54,61
 +3VA 20,38,41,54,59,63
 +3VSUS 18,21,22,23,28,29,30,51

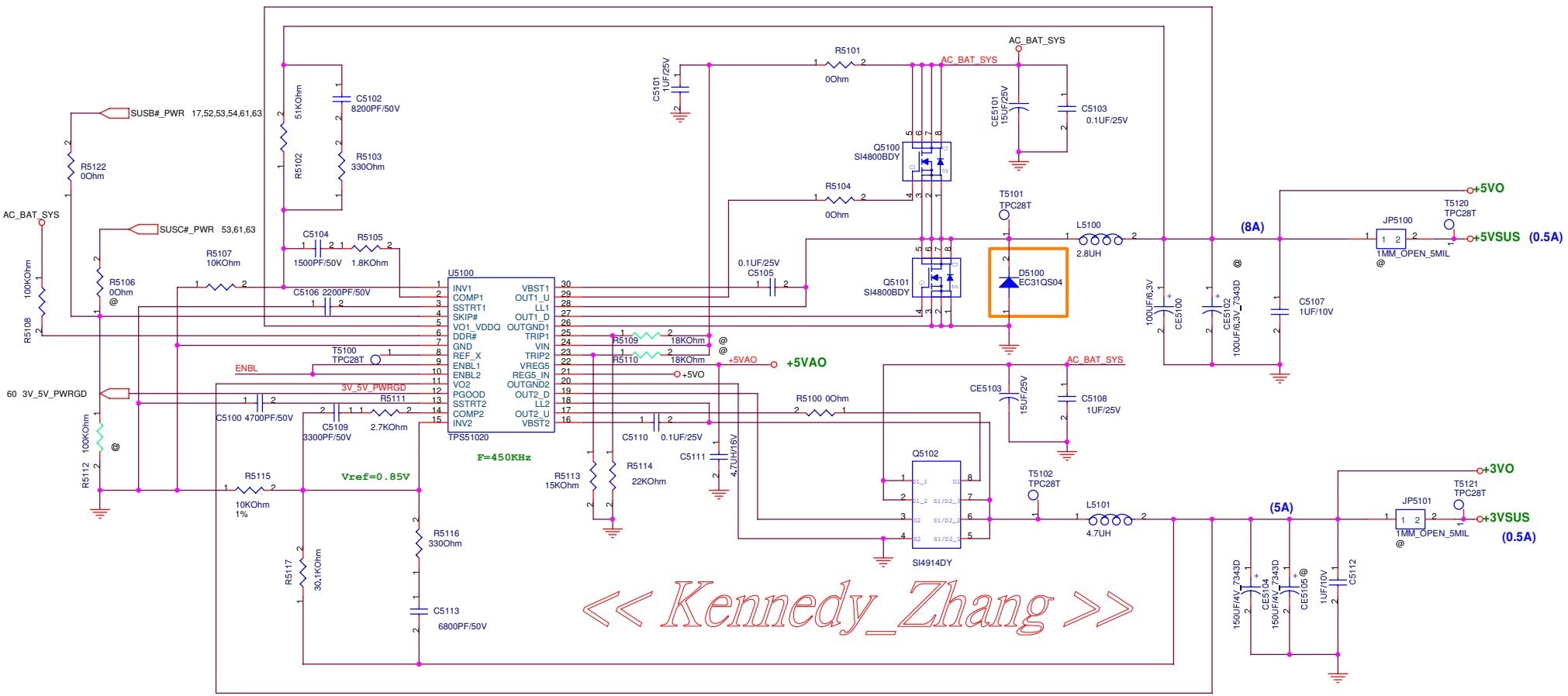




42.63 CPU_VRON
 22 PM DPRSLPVR
 4.20 H DPRSTP#
 7 CLK_EN#

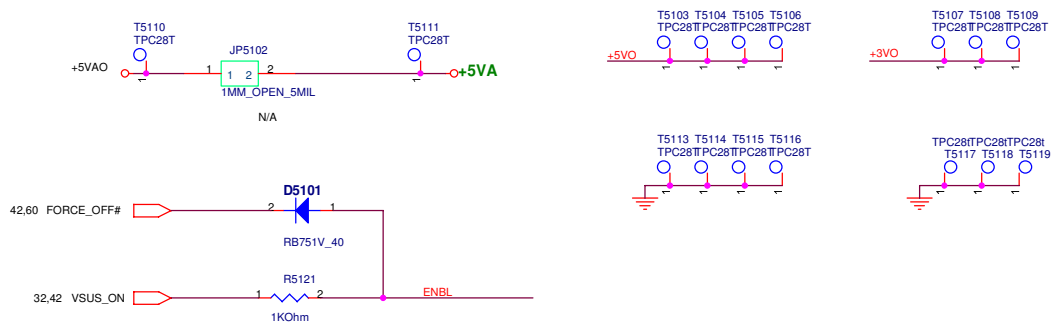
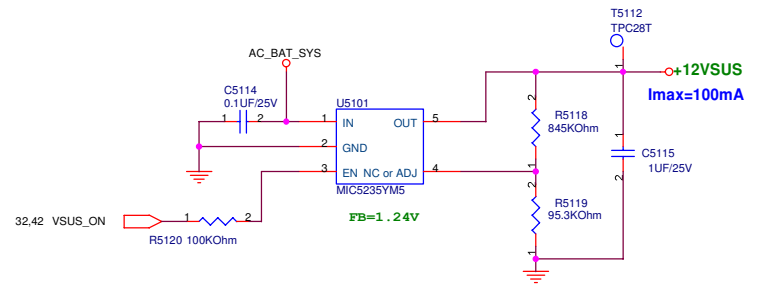
1 R5005 2 4990hm
 1 R5007 2 00hm
 1 R5009 2

Close to Phase 1 Inductor

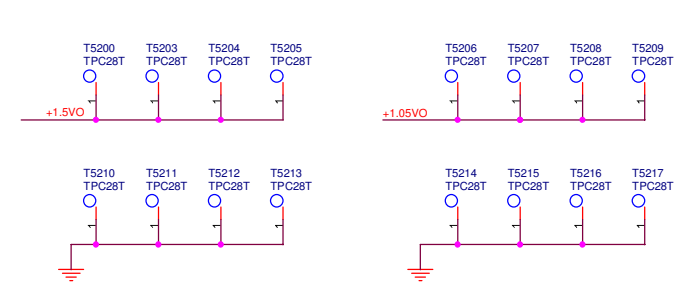
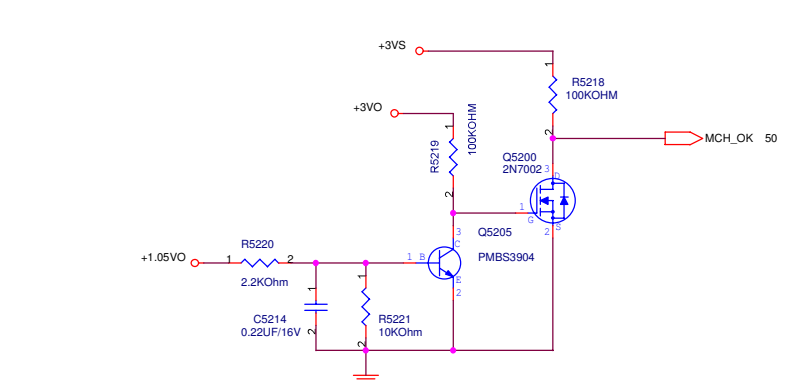
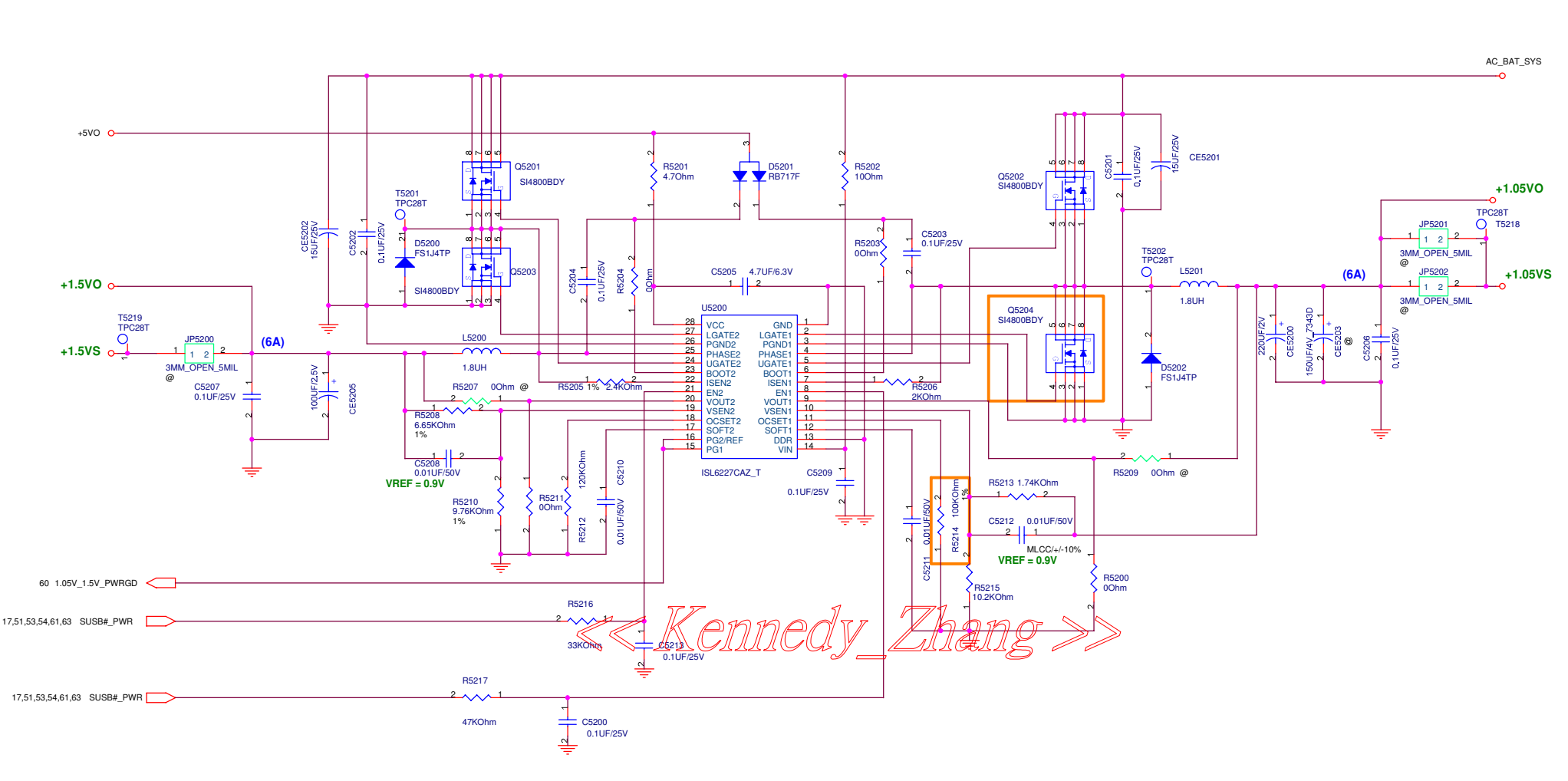


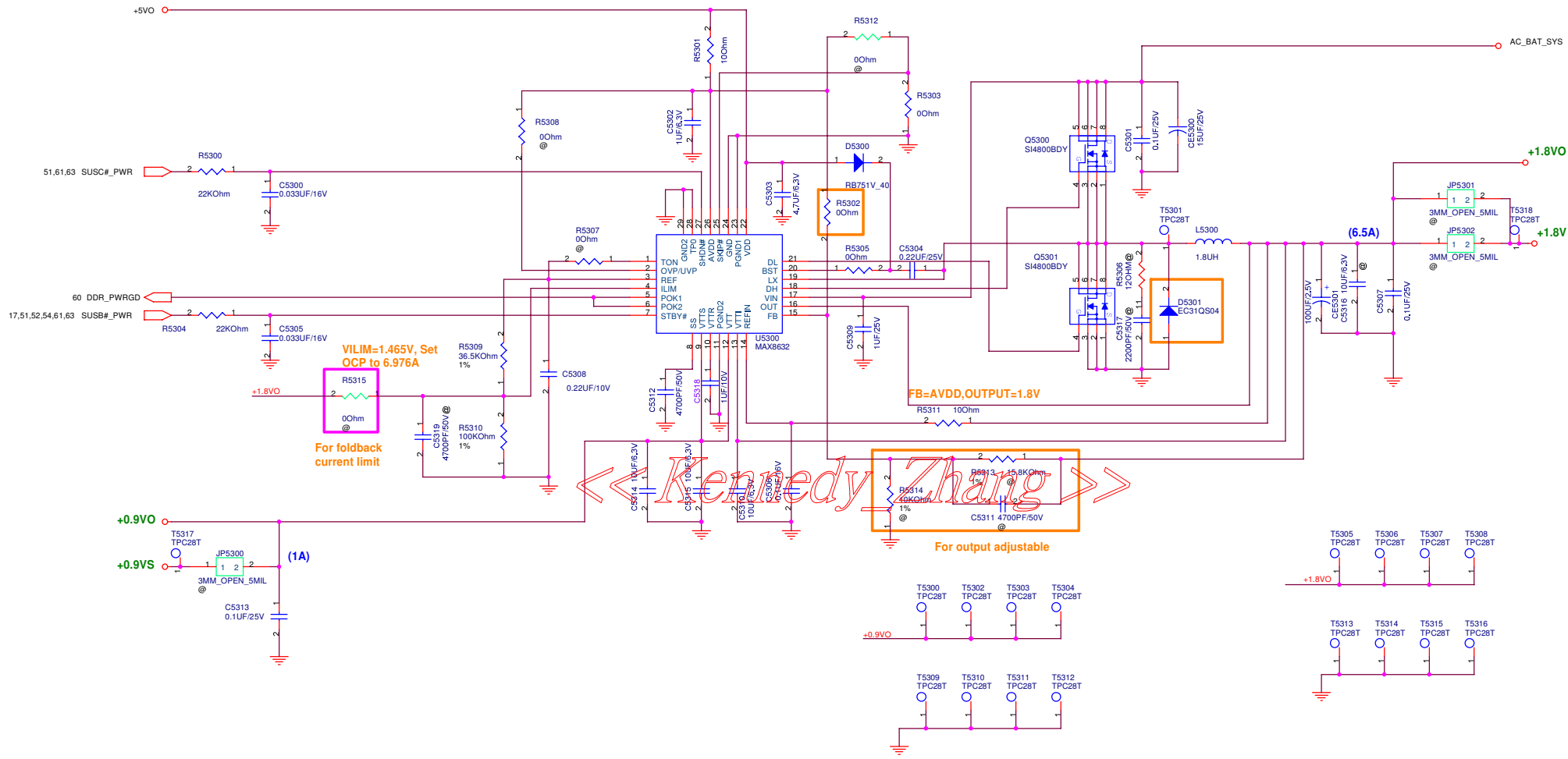
<< Kennedy_Zhang >>

+12VSUS

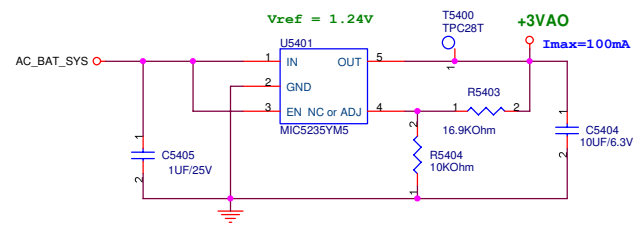
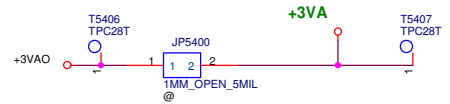


ASUS		Title : POWER_SYSTEM	
<OrgName>		Engineer: Mia / Charlse	
Size	Project Name	Rev	
Custom	A8J	2.0	
Date: Wednesday, March 29, 2006		Sheet	51 of 63



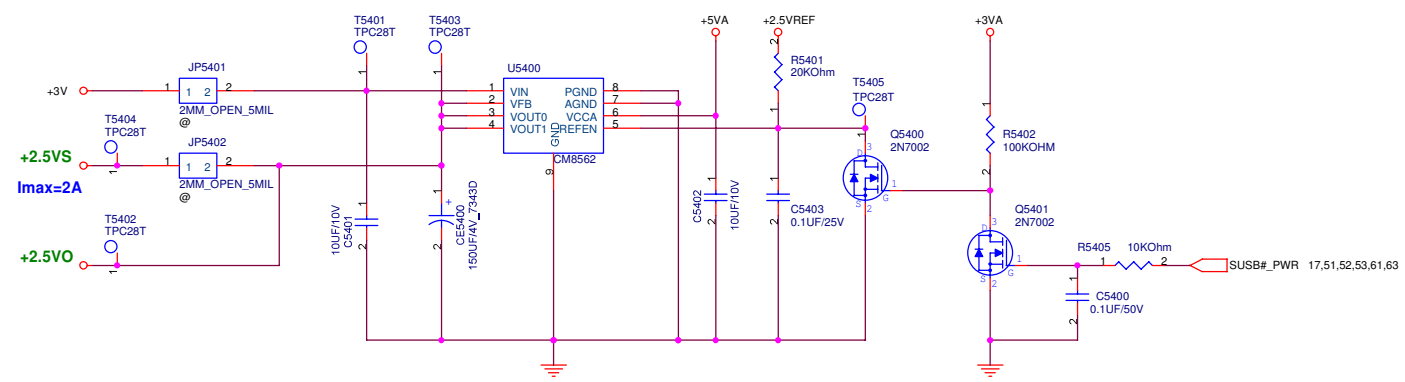


+3VAO

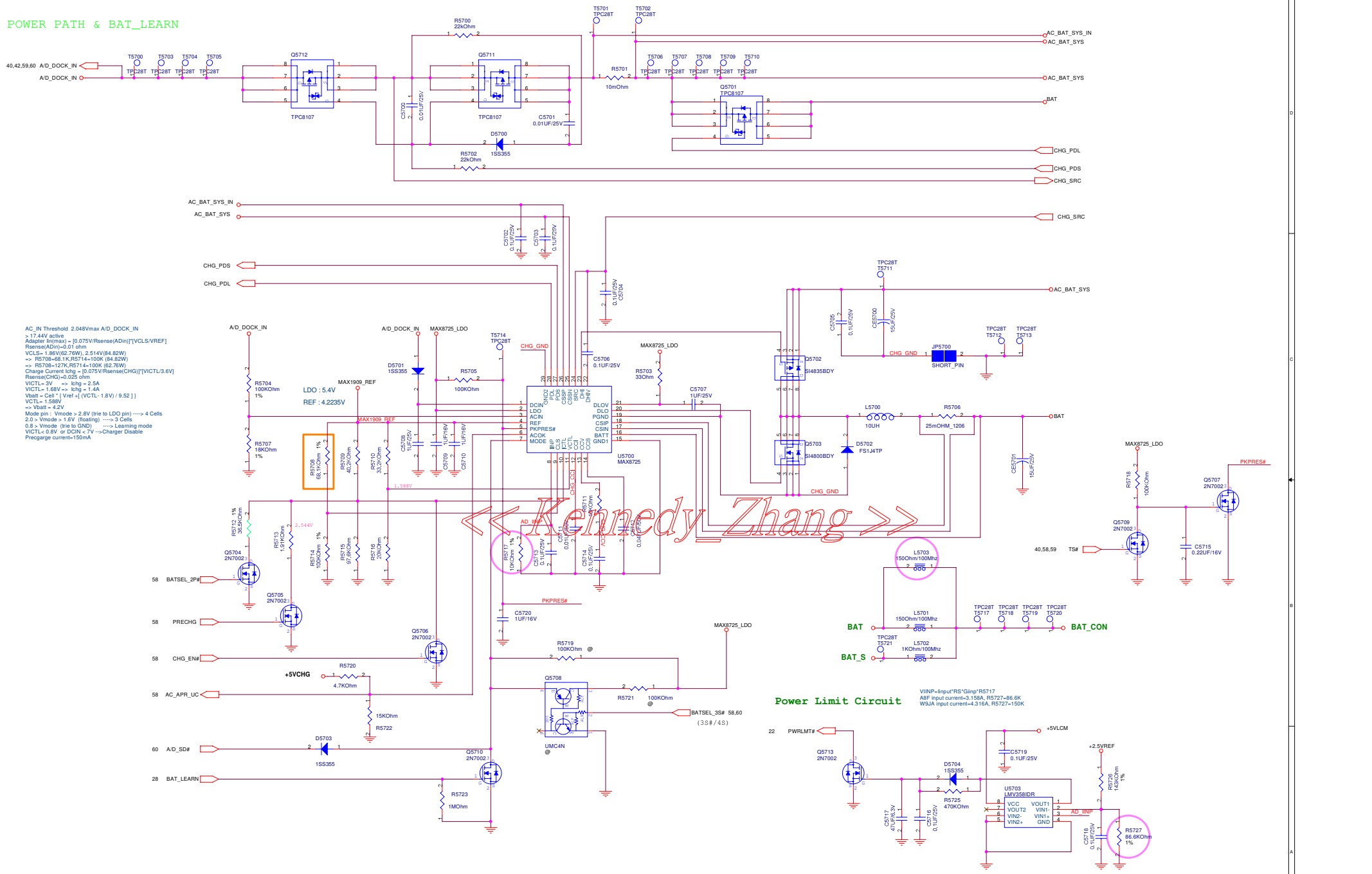


+2.5VS

<< Kennedy_Zhang >>



POWER PATH & BAT_LEARN

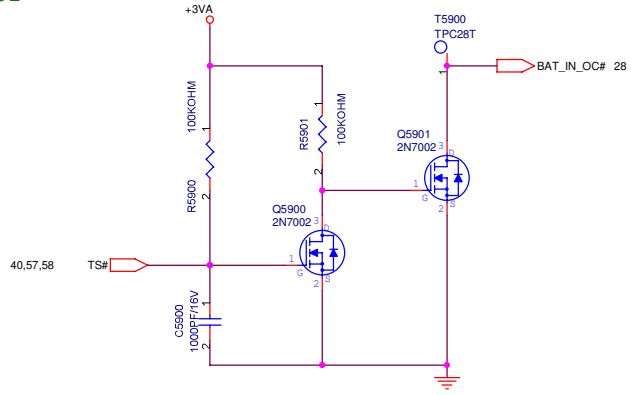


AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
Adapter In(max) = [0.075V/Rsense(ADin)]*(VCLS/VREF)
Rsense(ADin)=0.01 ohm
VCLS = 1.86V(62.76W), 2.514V(84.82W)
=> R5708=48.1K,R5714=100K(84.82W)
=> R5708=127K,R5714=100K(62.76W)
Charge Current Ichg = [0.075V/Rsense(CHG)]*(VICTL/3.6V)
Rsense(CHG)=0.025 ohm
VICTL = 3V -> Ichg = 2.5A
VICTL = 1.585V -> Ichg = 1.4A
Vbat = Cell * [Vref - (VICTL - 1.8V) / 9.52]
VCTL = 1.585V
=> Vbat = 4.2V
Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells
2.9 > Vmode > 1.6V (floating) -> 3 Cells
0.8 > Vmode (tie to GND) -> Learning mode
VICTL < 0.8V or DCHN < 7V -> Charger Disable
Precharge current=150mA

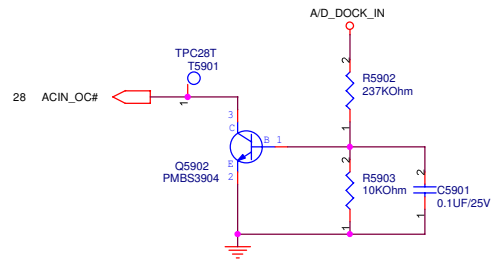
Power Limit Circuit

VINP=Input'RS'Gimp'R5717
ABF input current=3.158A, R5727=86.6K
WJA input current=4.316A, R5727=159K

BATTERY IN DETECT

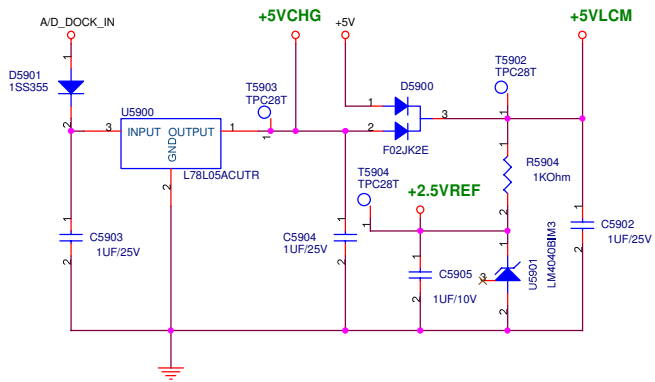


ADAPTER IN DETECT

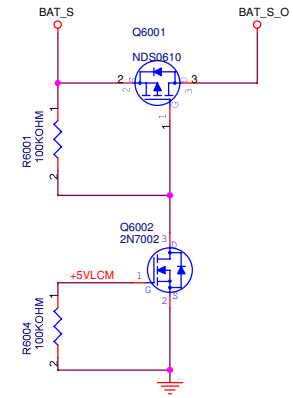
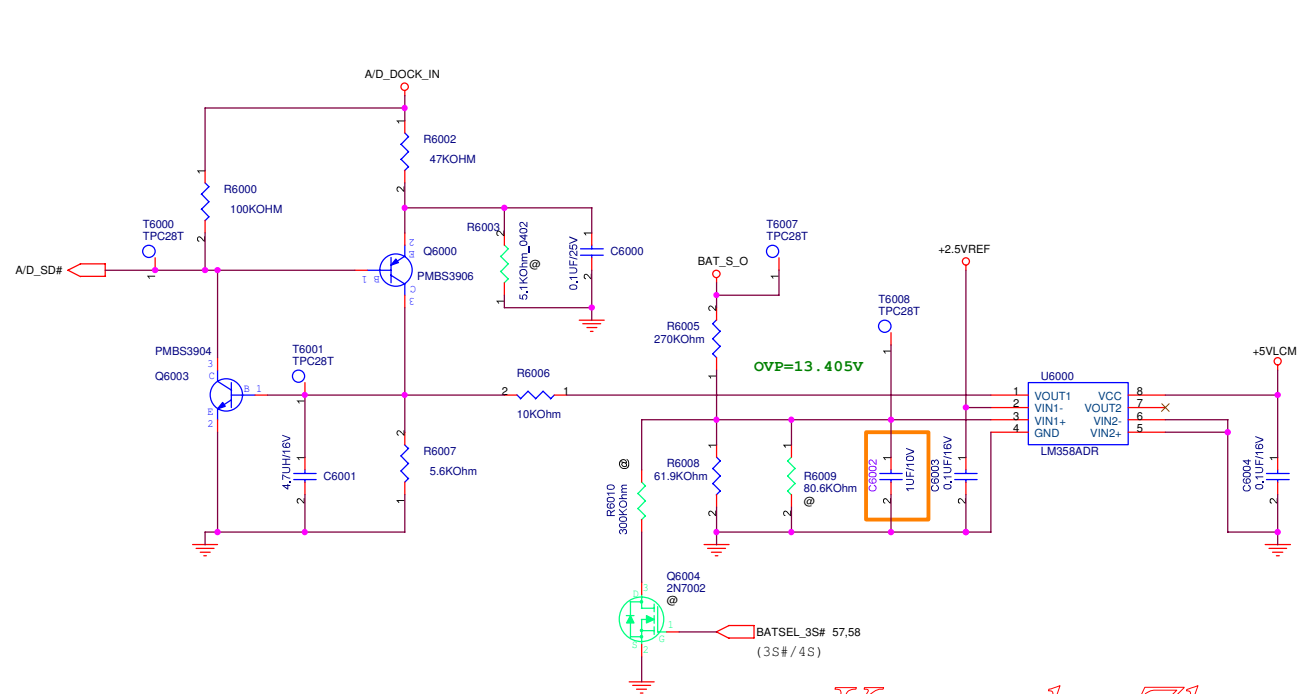


+5VLCM, +5VCHG & +2.5VREF

<< Kennedy_Zhang >>

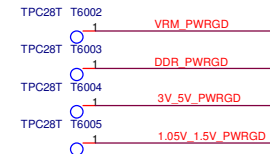
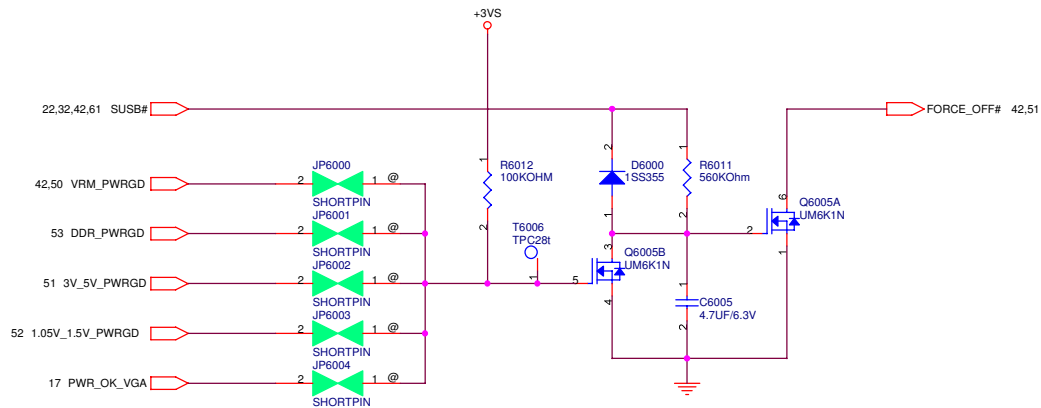


BATTERY A/D_SD# (OVP)

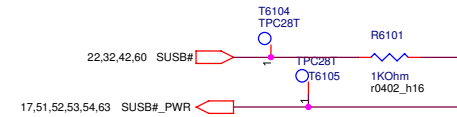
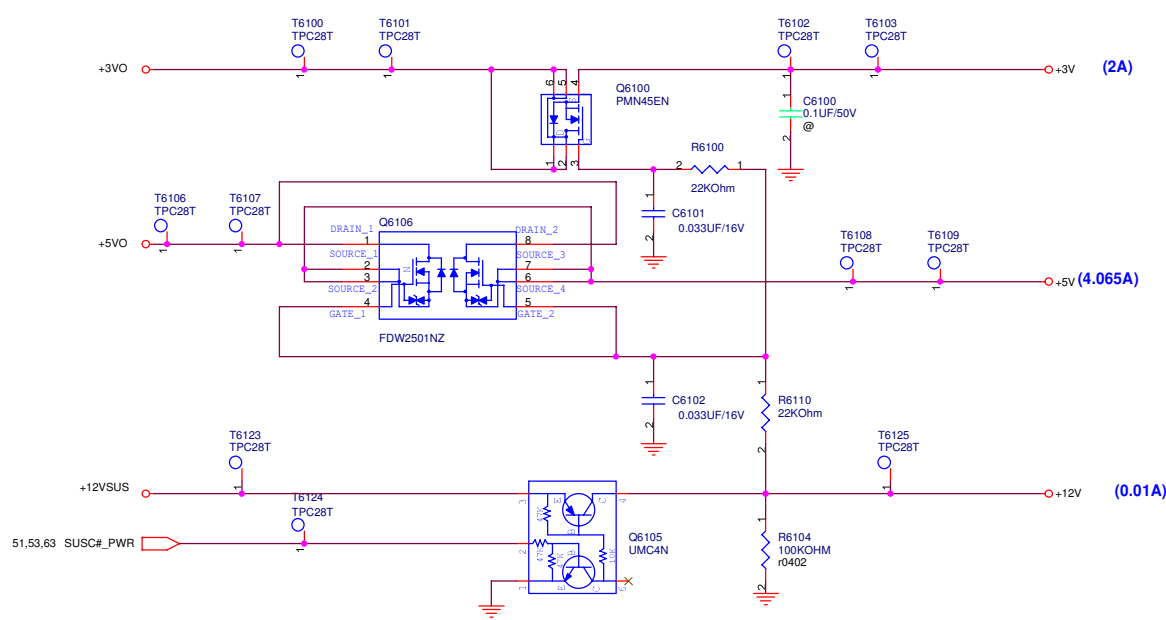


<< Kennedy_Zhang >>

POWER GOOD DETECTOR

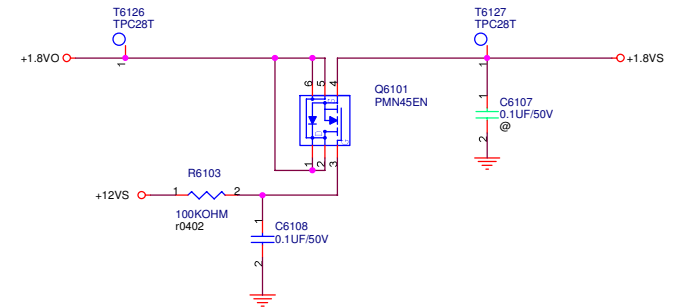
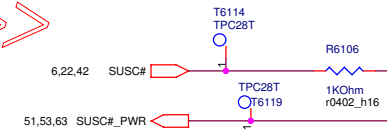
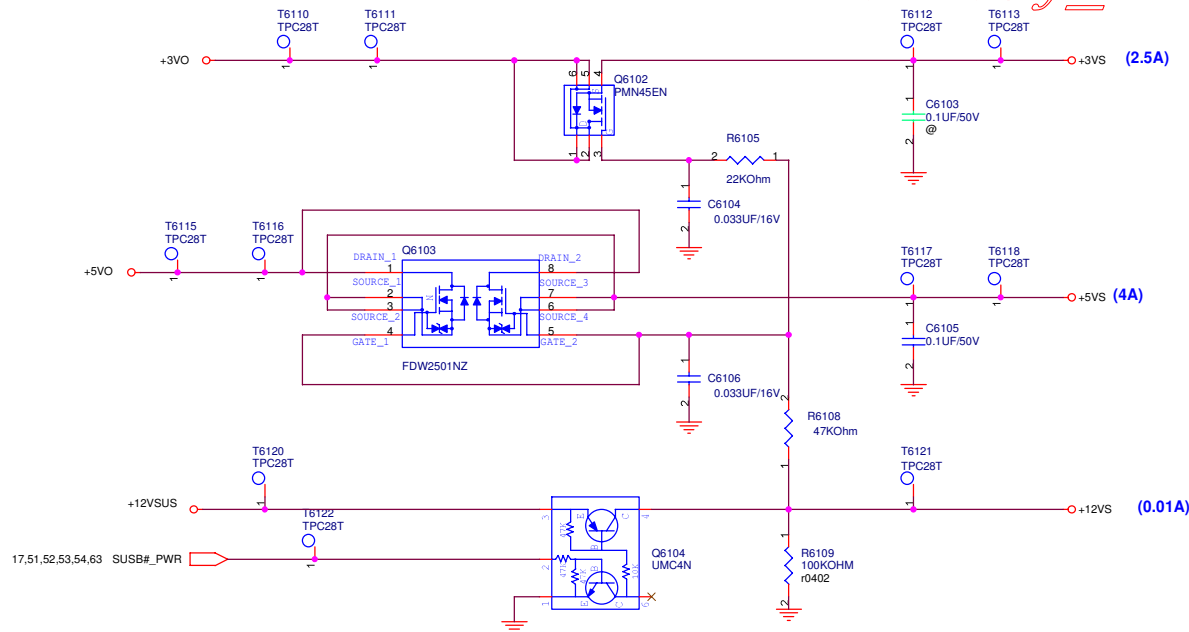


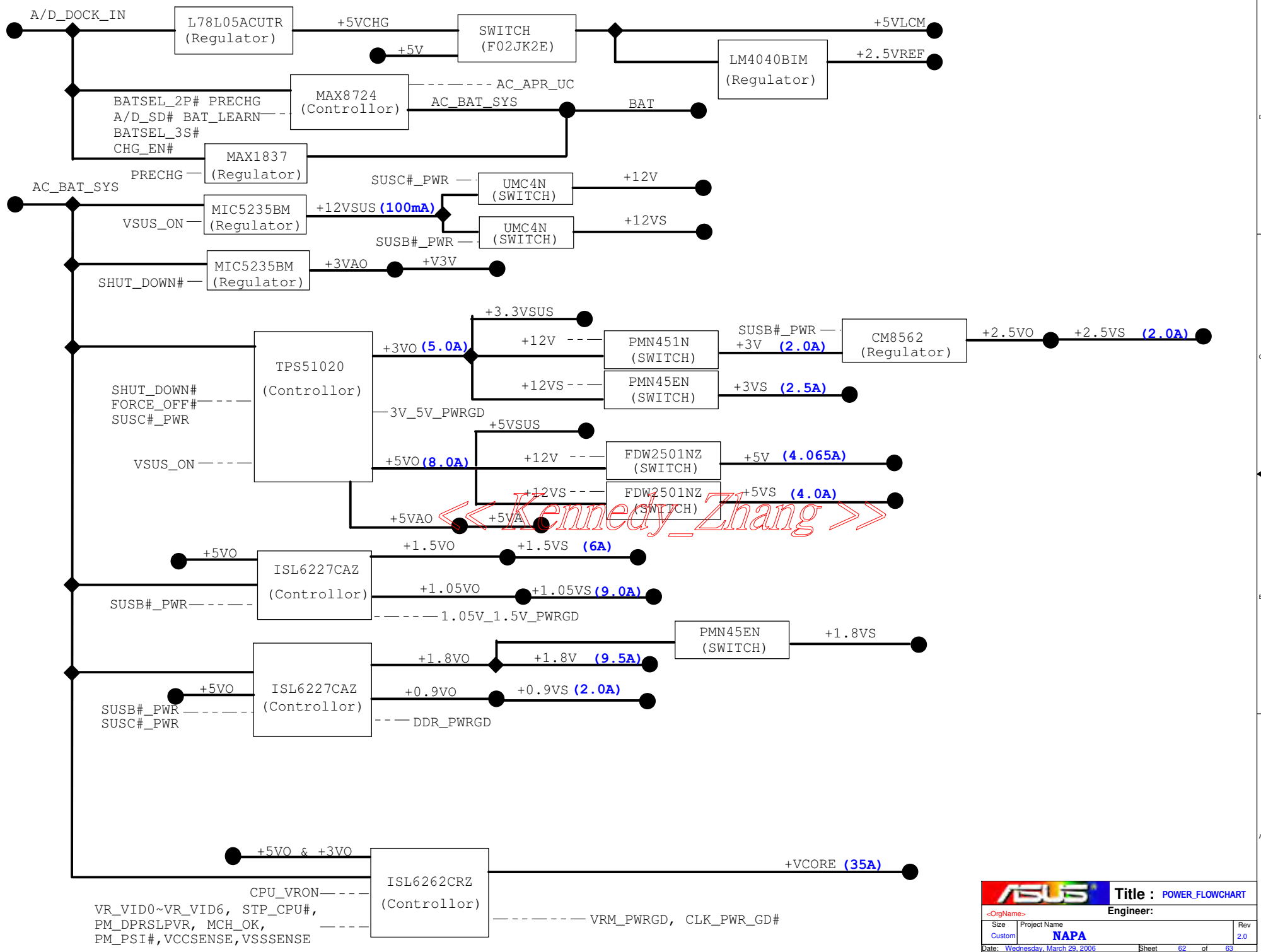
SUSC#_PWR POWER



SUSB#_PWR POWER

<< Kennedy_Zhang >>

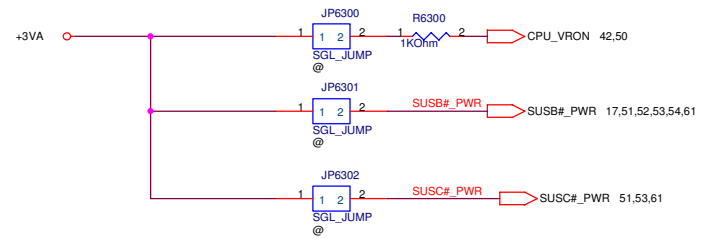




« Kennedy_Zhang »

AC_BAT_SYS	→	AC_BAT_SYS	17,18,50,51,52,53,54,57
+3VA	→	+3VA	20,38,41,42,54,59
+5VA	→	+5VA	6,51,54
+5VO	→	+5VO	51,52,53,61
+3VO	→	+3VO	51,52,61
+3V	→	+3V	28,30,31,32,34,37,38,42,54,61
+3VS	→	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+12VSUS	→	+12VSUS	51,61
+12V	→	+12V	25,34,37,40,61
+12VS	→	+12VS	17,18,41,61
+5V	→	+5V	15,17,19,25,28,32,36,38,40,41,59,61
+5VS	→	+5VS	19,22,23,24,28,29,36,37,38,39,40,41,50,61
+2.5VO	→	+2.5VO	54
+2.5VS	→	+2.5VS	11,17,19,38,54
+1.8VO	→	+1.8VO	53,61
+1.8V	→	+1.8V	9,12,14,15,38,53
+1.8VS	→	+1.8VS	17,61
+0.9VS	→	+0.9VS	16,17,53
BAT	→	BAT	57
+5VCHG	→	+5VCHG	57,59
+5VLCM	→	+5VLCM	28,57,58,59,60
+2.5VREF	→	+2.5VREF	54,57,59,60
+VCORE	→	+VCORE	5,6,50
+VGA_VCORE	→	+VGA_VCORE	
+VRAM	→	+VRAM	
+1.2VSP	→	+1.2VSP	

FOR POWER TEST



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