

GIGABYTE GA-8IPE1000-G

Schematics

Revision 3.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3,4 CHANNEL B
13	DDR TERMINATION
14	AGP 8X SLOT
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	DUAL FWH
19	ICS952635 CLOCK GENERATOR
20	PCI SLOT1/SLOT2
21	PCI SLOT3/SLOT4/RESET BUFFER
22	PCI SLOT5/SLOT6

SHEET

TITLE

23	AC '97 CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712/IR_CIR/SCR/S_IRQ
26	COMA/VGA_COMB/LPT
27	IDE1/IDE2/FDD
28	FAN/HW MONITOR
29	KB_MS/GAME/FUSEVCC
30	FRONT PANEL
31	R_USB/F_USB1/F_USB2
32	DDR/VDDQ/5VDUAL/VCCVID POWER
33	VCORE POWER
34	ATX/ATX_12V/FAN1655M
35	MARVELL 88E8001
36	TI TSB43AB23(1394)
37	PCI ROUNTIONG
38	GPIO PIN LIST

PROCESS: C

COMPONENT SIDE
(0.5 oz. Copper)

VCC SIDE
(1 oz. Copper)

GND SIDE
(1 oz. Copper)

SOLDER SIDE
(0.5 oz. Copper)

GIGABYTE CORP.

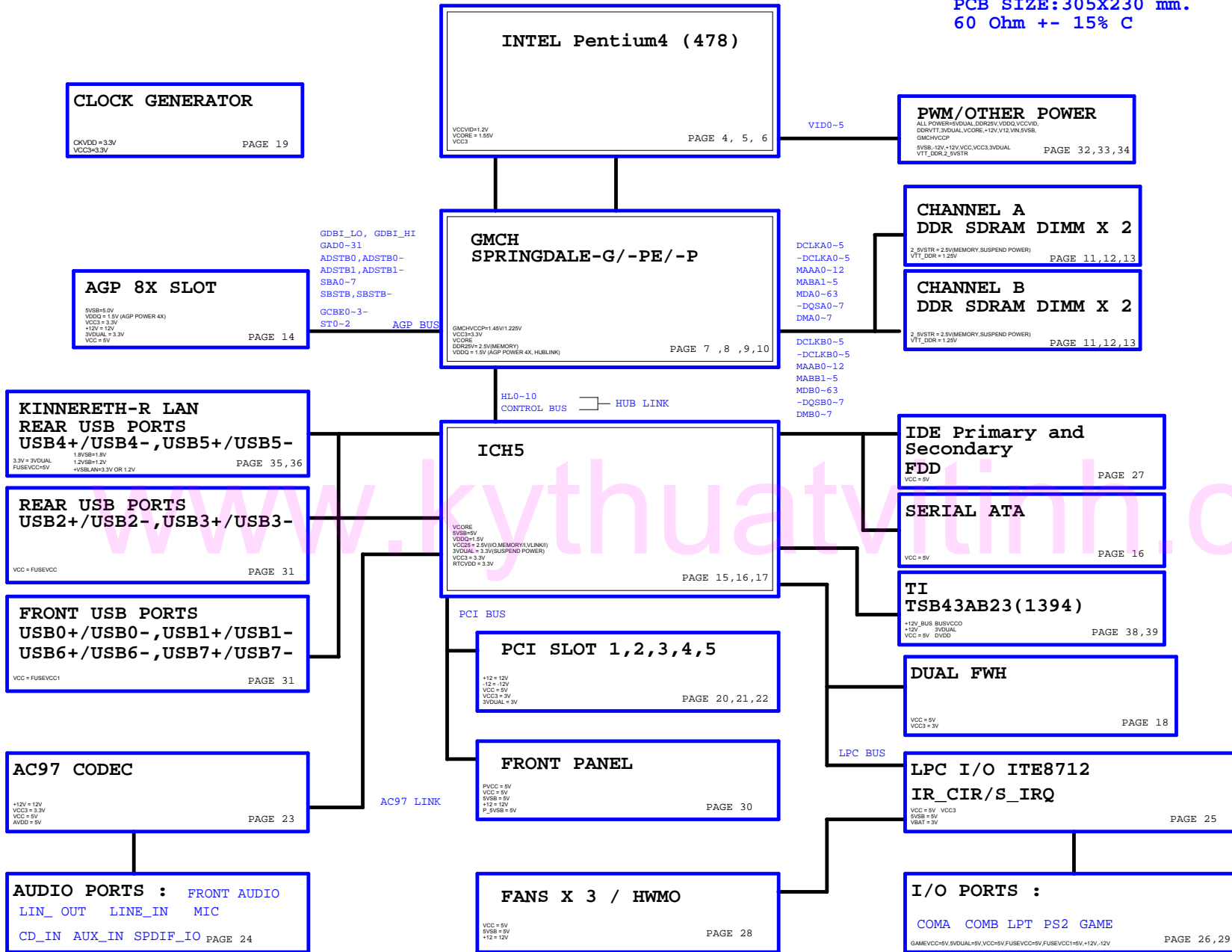
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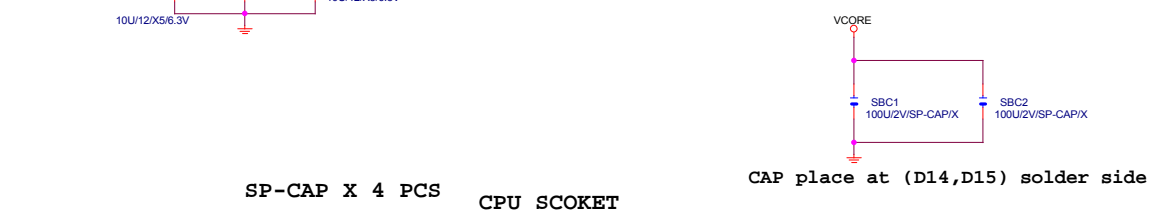
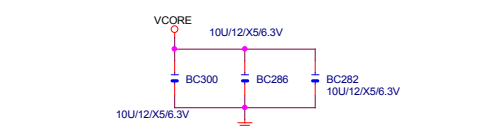
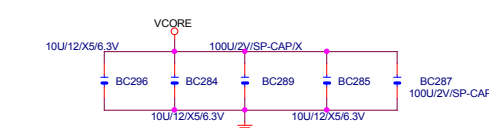
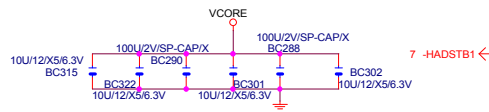
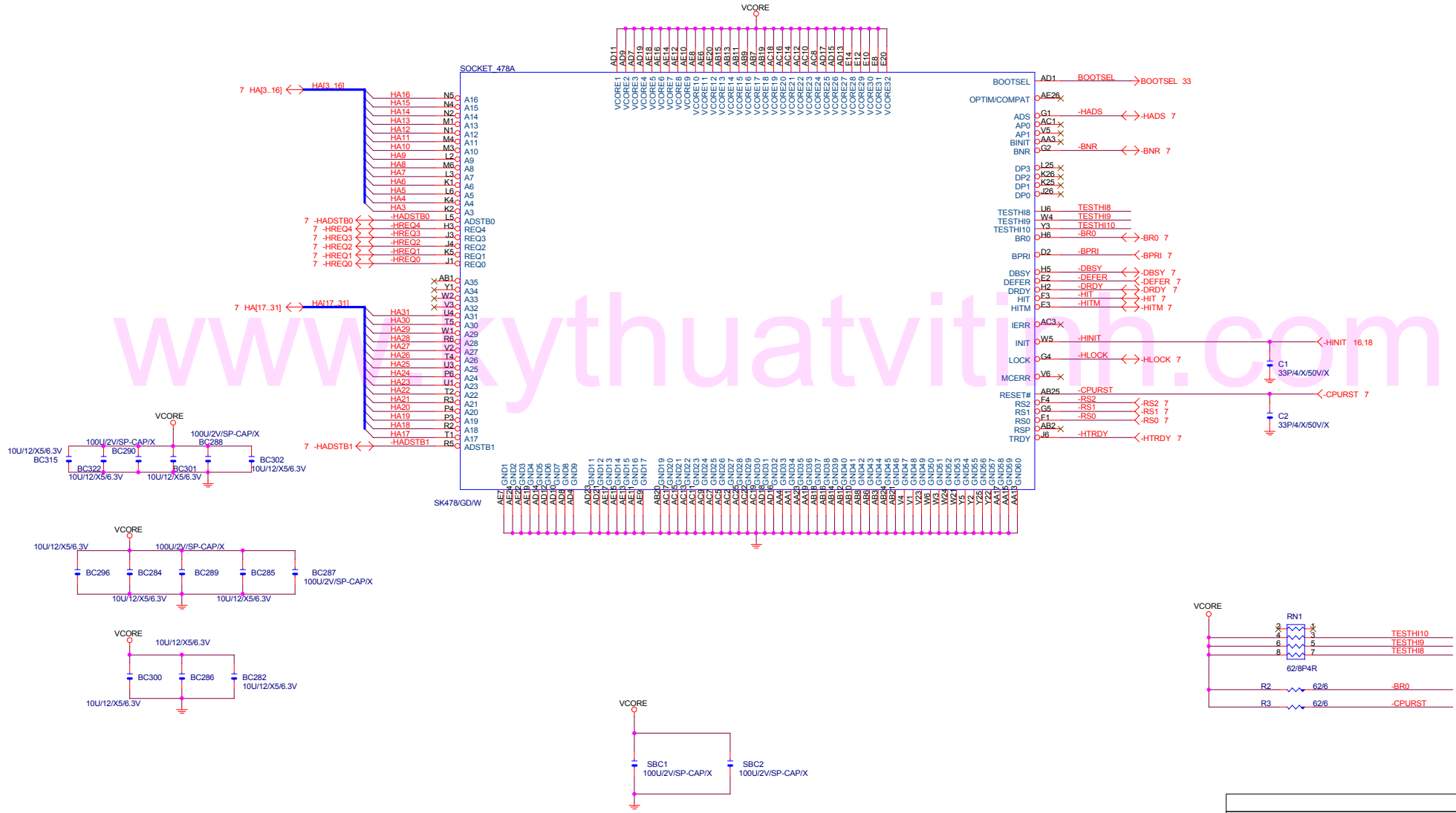
Size: Custom Document Number: GA-8IPE1000-G Rev: 3.0

Date: Sheet 1 of 38

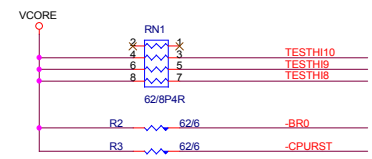
BLOCK DIAGRAM

PCB SIZE: 305X230 mm.
60 Ohm +/- 15% C

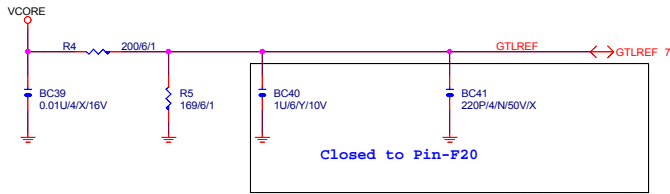




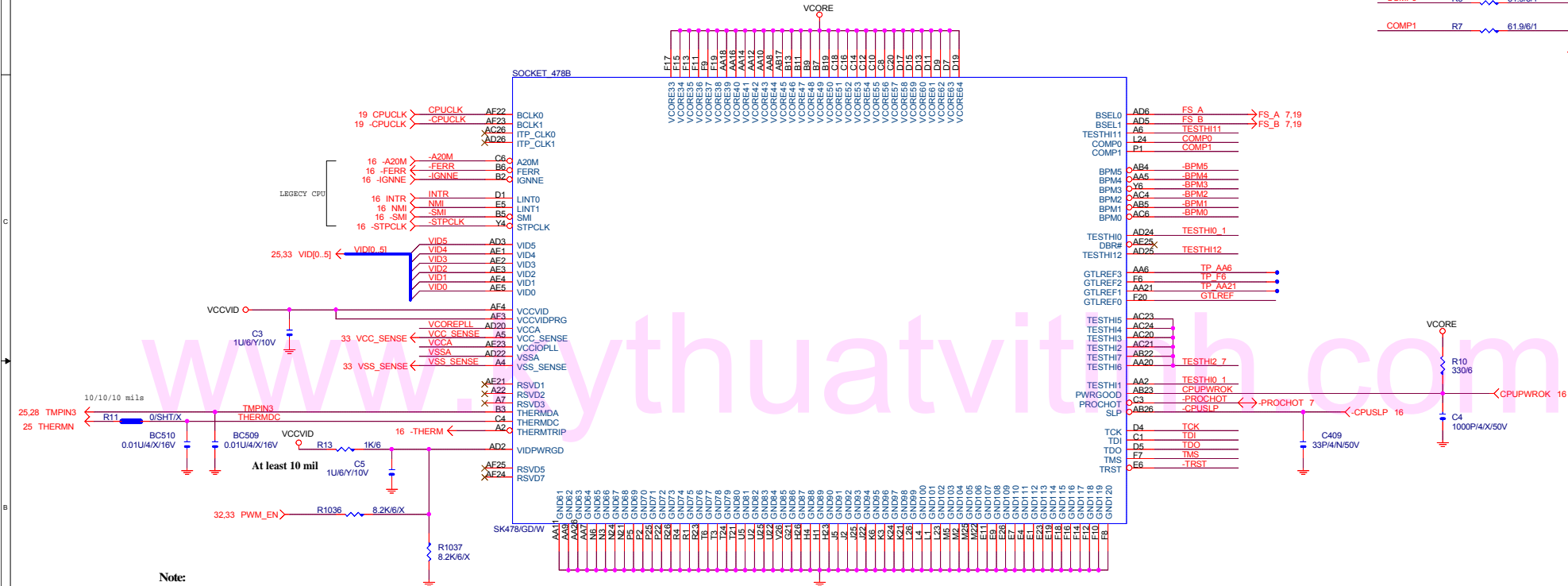
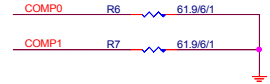
SP-CAP X 4 PCS CPU SCKET



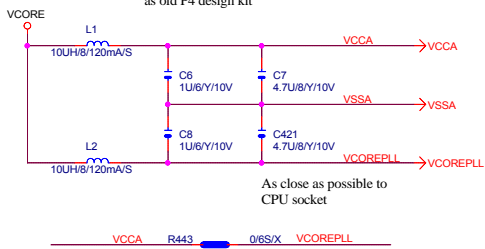
Title		
P4 478A		
Size	Document Number	Rev
Custom	GA-8IPE1000-G	3.0
Date:	Sheet	4 of 38



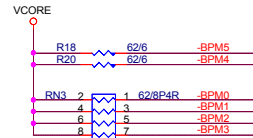
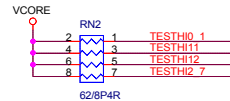
Place outside of CPU socket



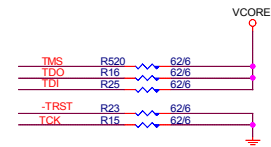
Note:
VCCA & VCCOREPLL define doesn't same as old P4 design kit



As close as possible to CPU socket



Close to CPU

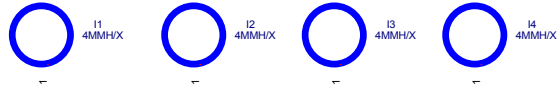
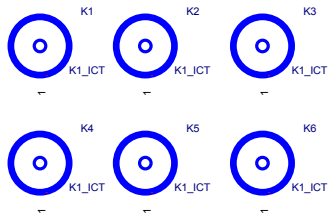


Close to CPU

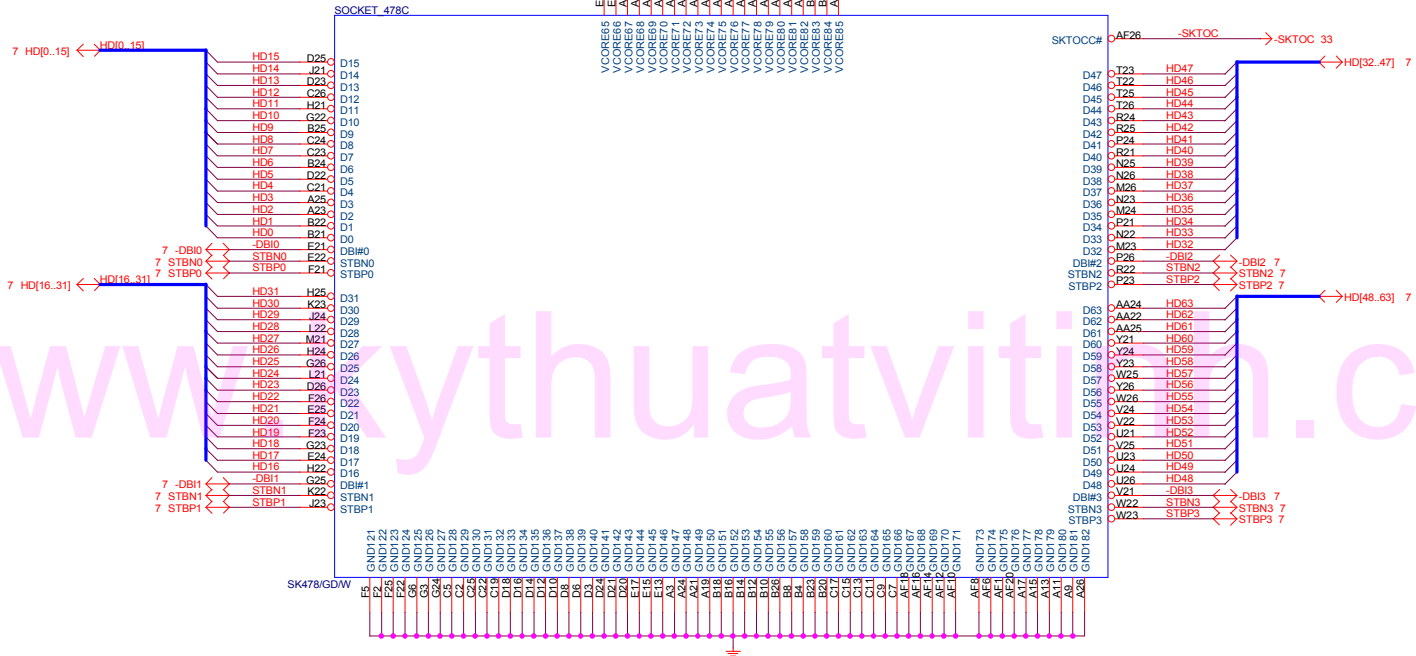
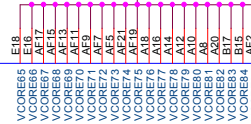


Pull up must place end of route

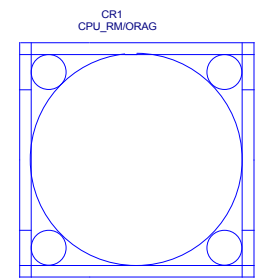
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P4 478B		
Size	Document Number	Rev
Custom	GA-8IPE1000-G	3.0
Date:	Sheet	5 of 38



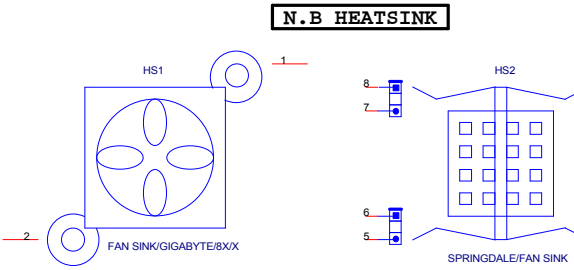
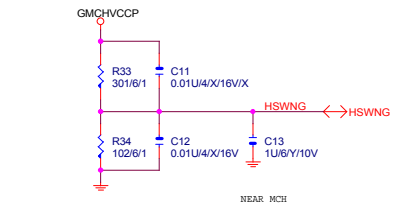
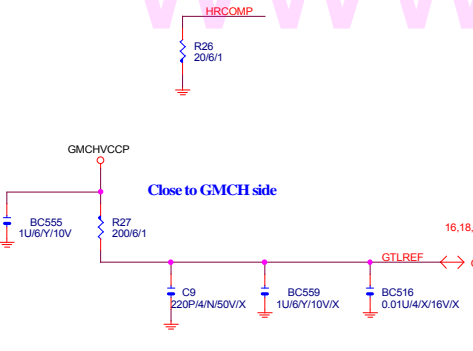
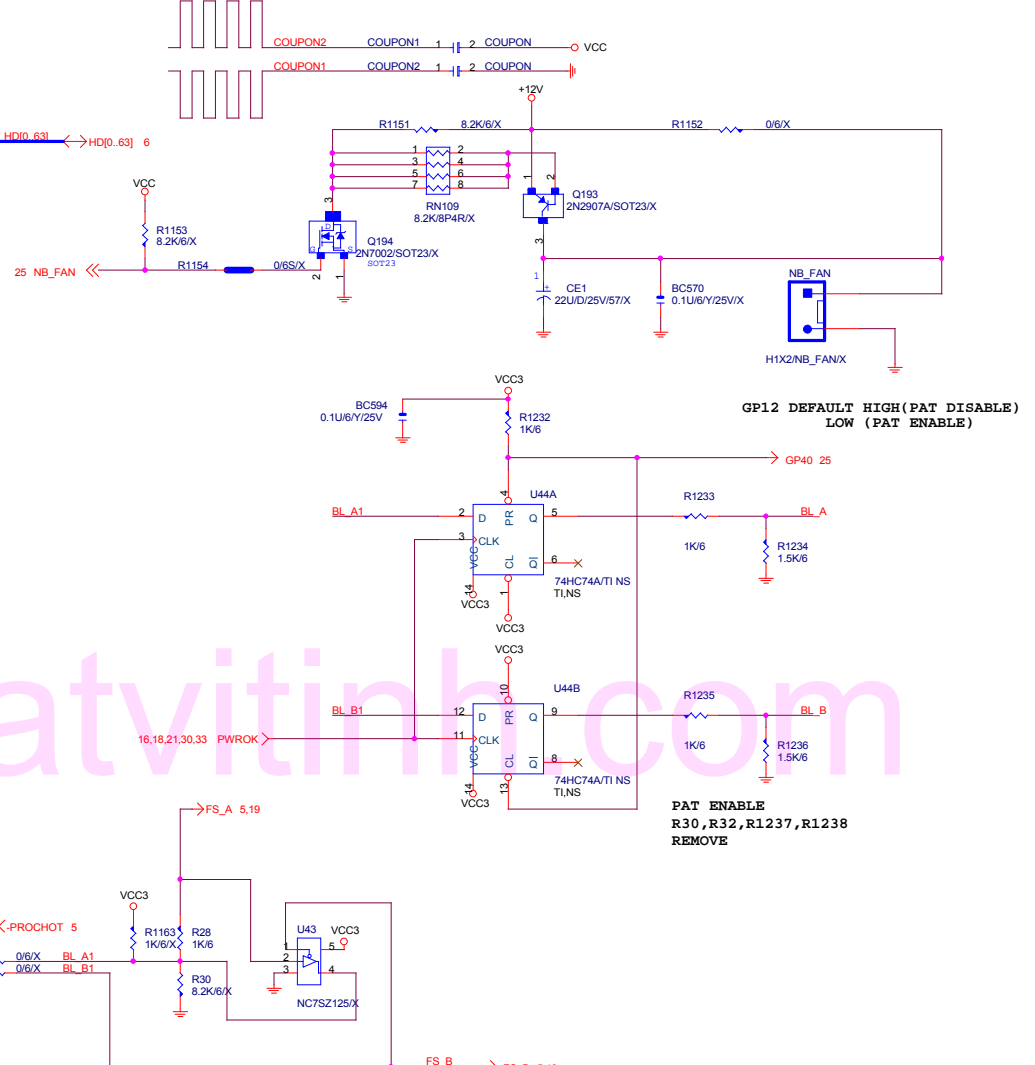
VCORE



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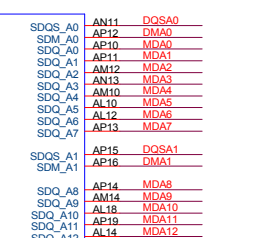
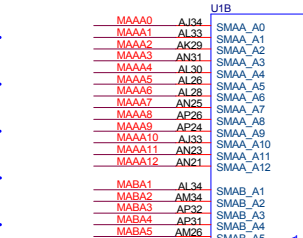
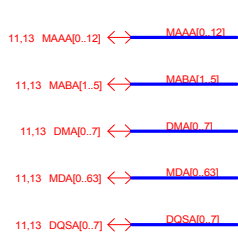
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Size	Document Number				Rev
Custom	GA-8IPE1000-G				3.0
Date:	Sheet 6 of 38				



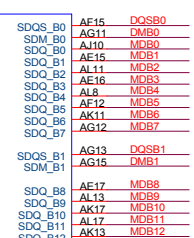
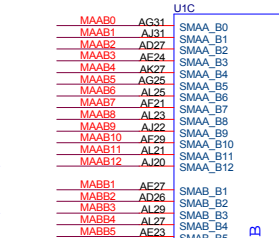
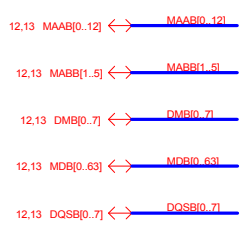
	100	133	200
FS_A	L	H	L
FS_B	L	L	H
X2 (NO)	X2	X2	X1.33
	X2.66	X2.5	X1.6
			X2

FOR SPD P (533MHZ)
REMOVE R28,R31
ADD R1163,U39,

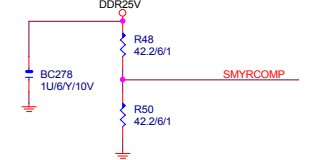
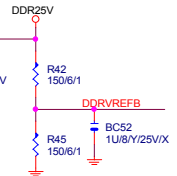
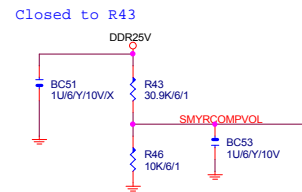
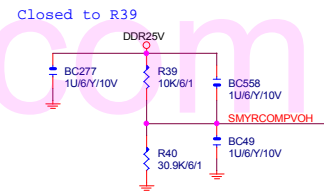
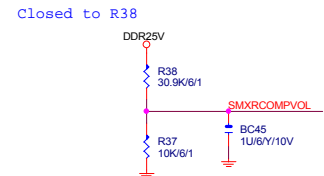
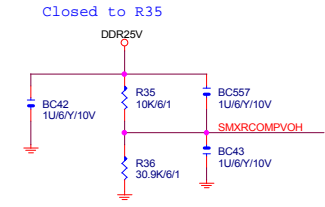
DDR 400 1-2-3-4 CPC DISABLE
 DDR 333 SIGNAL 1 CPC ENABLE
 2 CPC DISABLE
 DUAL 2 CPC ENABLE
 DUAL 4 CPC DISABLE



DDR Channel A



DDR Channel B



Title		
SPRINGDALE DDR		
Size	Document Number	Rev
Custom	GA-8IPE1000-G	3.0
Date:	Sheet	8 of 38

14 GAD[0..31] <-> GAD[0..31]
 14 SBA[0..7] <-> SBA[0..7]
 15 HL[0..10] <-> HL[0..10]

UIID
 14 -GCBE0 <-> -GCBE0 Y7 GCBE0 GADSTBF0 AC6 ADSTB0 <-> ADSTB0 14
 14 -GCBE1 <-> -GCBE1 W5 GCBE1 GADSTBF0 AC5 ADSTB0 <-> ADSTB0 14
 14 -GCBE2 <-> -GCBE2 AA3 GCBE2 GADSTBF0 AC5 ADSTB0 <-> ADSTB0 14
 14 -GCBE3 <-> -GCBE3 U2 GCBE3 GADSTBF0 AC5 ADSTB0 <-> ADSTB0 14

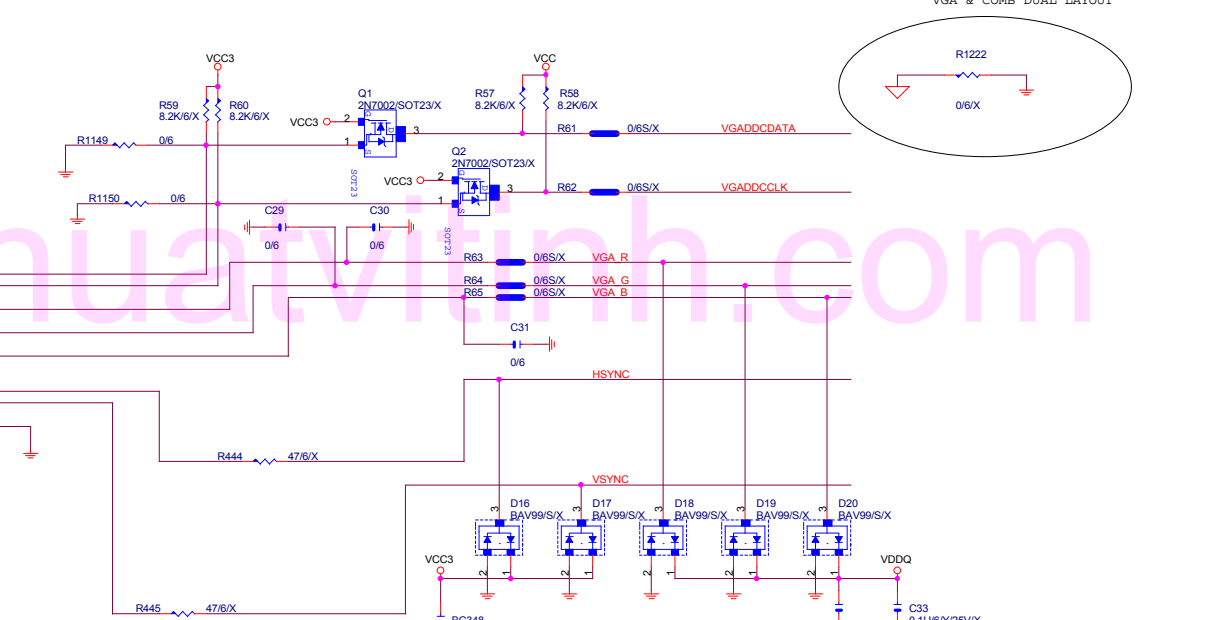
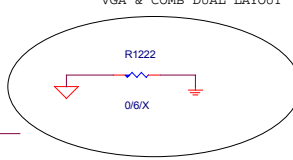
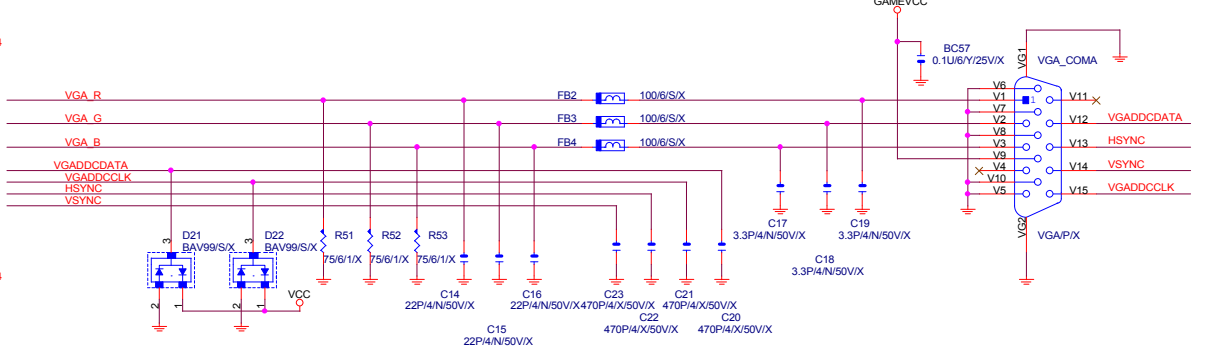
AGP
 14 -GFRAME <-> -GFRAME U6 GFRAME GAD0 AE6 GAD0
 19 GMCH3V66 <-> GMCH3V66 M4 GCLKIN GAD1 AC11 GAD1
 14 -GDEVSEL <-> -GDEVSEL AB4 GDEVSEL GAD2 AD5 GAD2
 14 -GIRDY <-> -GIRDY V11 GIRDY GAD3 AE5 GAD3
 14 -GTRDY <-> -GTRDY AB5 GTRDY GAD4 AA10 GAD4
 14 -GSTOP <-> -GSTOP W11 GSTOP GAD5 AC9 GAD5
 14 -GPAR <-> -GPAR AB2 GPAR GAD6 AB11 GAD6
 14 -GREQ <-> -GREQ M6 GREQ GAD7 AB7 GAD7
 14 -GGNT <-> -GGNT N7 GGNT GAD8 AA9 GAD8
 14 -GPAR_ADD_DETECT <-> GPAR_ADD_DETECT GAD9 AA6 GAD9
 14 -GRCOMP <-> -GRCOMP AC2 GRCOMP GAD10 AA5 GAD10
 14 -GSWING <-> -GSWING AC3 GSWING GAD11 W10 GAD11
 14 MCH_AGPREF <-> MCH_AGPREF AD2 GVRREF GAD12 W6 GAD12
 14 -RBF <-> -RBF R10 GRBF GAD13 W9 GAD13
 14 -WBF <-> -WBF R9 GWBF GAD14 W7 GAD14
 14 -PIPE <-> -PIPE M4 DBL_HI GAD15 V7 GAD15
 14 GDBI_LO <-> GDBI_LO M5 DBL_LO GAD16 AA2 GAD16

HUB
 14 ST0 <-> ST0 N3 GST0 GAD17 Y4 GAD17
 14 ST1 <-> ST1 N2 GST1 GAD18 Y2 GAD18
 14 ST2 <-> ST2 N2 GST2 GAD19 W2 GAD19
 14 ST1 <-> ST1 N2 GST1 GAD19 W2 GAD19
 14 ST2 <-> ST2 N2 GST2 GAD19 W2 GAD19
 14 ST1 <-> ST1 N2 GST1 GAD19 W2 GAD19
 14 ST2 <-> ST2 N2 GST2 GAD19 W2 GAD19

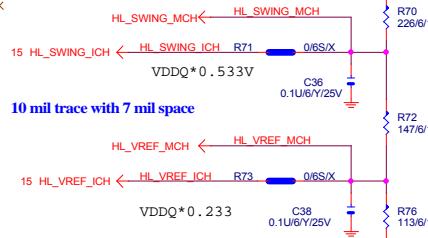
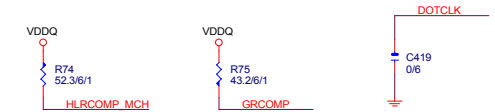
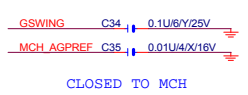
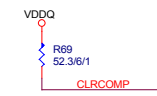
CSA
 15 HLSTBF <-> HLSTBF AH5 HISTRF GSBSTBF LH1 SBSTB <-> SBSTB 14
 15 HLSTBS <-> HLSTBS AH4 HISTRF GSBSTBS T11 SBSTB <-> SBSTB 14
 15 HLSTBF <-> HLSTBF AH5 HISTRF GSBSTBF LH1 SBSTB <-> SBSTB 14
 15 HLSTBS <-> HLSTBS AH4 HISTRF GSBSTBS T11 SBSTB <-> SBSTB 14

VGA
 10 CLSWING_SPG <-> CLSWING_SPG AF2 CLRCOMP AG2 HL_SWING_MCH AG3 HL_SWING_MCH AG3
 10 CLVREF_SPG <-> CLVREF_SPG AF4 CLRREF_SPG AG4 HL_VREF_MCH AG2 HL_VREF_MCH AG2
 19 DOTCLK <-> DOTCLK G4 DREFCLK EX1TSM AP8 TP_GMCH AG9 AG9
 16 -JCHSYNC <-> -JCHSYNC AJ8 -PCIRST <-> -PCIRST AK4 TP_GMCH AG10 AG10
 15,18,21,25,35,36 -PCIRST <-> -PCIRST AK4 TP_GMCH AG9 AG9

RESERVED
 RESERVED_1 NC_1 A3
 RESERVED_2 NC_2 A33
 RESERVED_3 NC_3 A35
 RESERVED_4 NC_4 AF13
 RESERVED_5 NC_5 AF23
 RESERVED_6 NC_6 AJ12
 RESERVED_7 NC_7 AN1
 RESERVED_8 NC_8 AP2
 RESERVED_9 NC_9 AR33
 RESERVED_10 NC_10 AR35
 RESERVED_11 NC_11 B2
 RESERVED_12 NC_12 B25
 RESERVED_13 NC_13 B34
 RESERVED_14 NC_14 C1
 RESERVED_15 NC_15 C23
 RESERVED_16 NC_16 C25
 RESERVED_17 NC_17 E26
 RESERVED_18 NC_18 M31
 RESERVED_19 NC_19 M31
 RESERVED_20 NC_20 R25



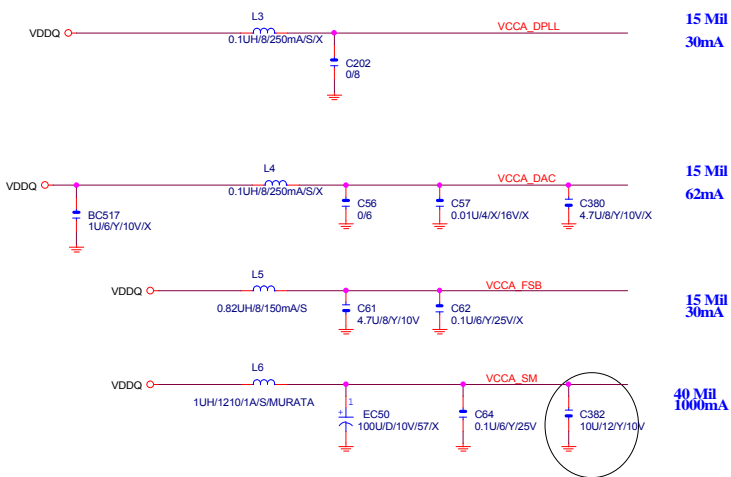
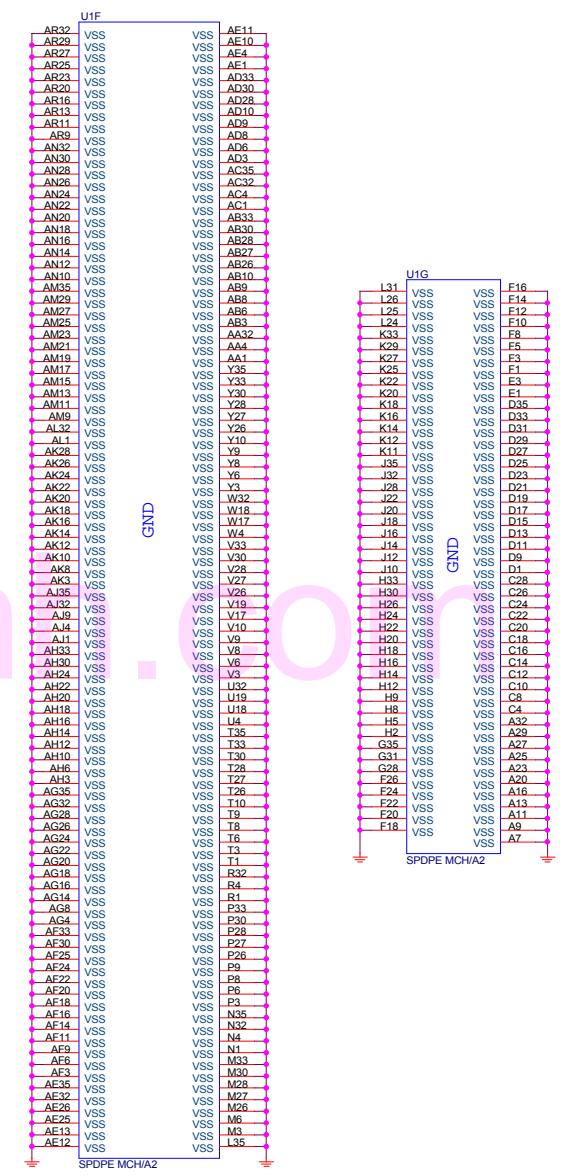
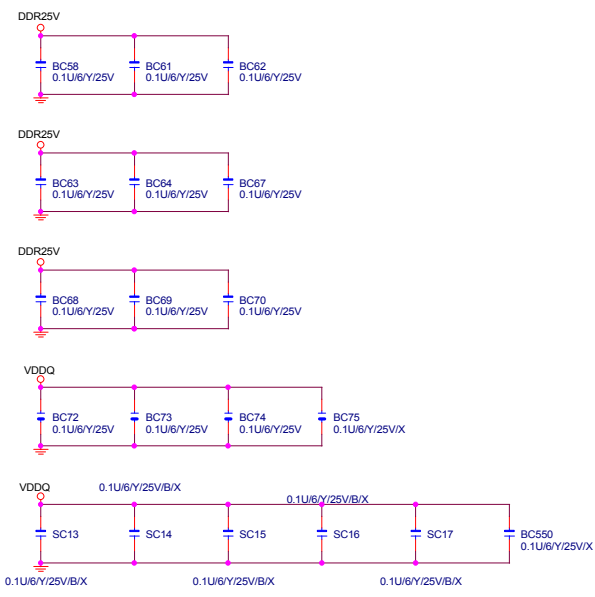
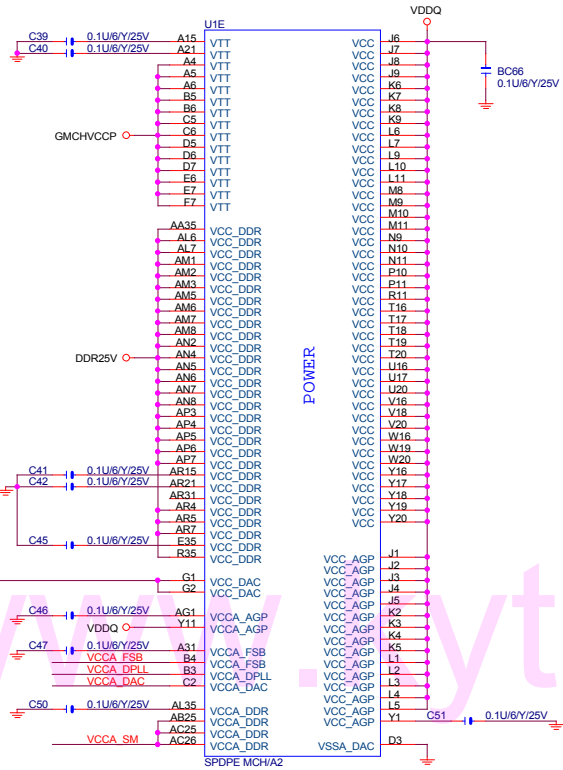
Close to MCH



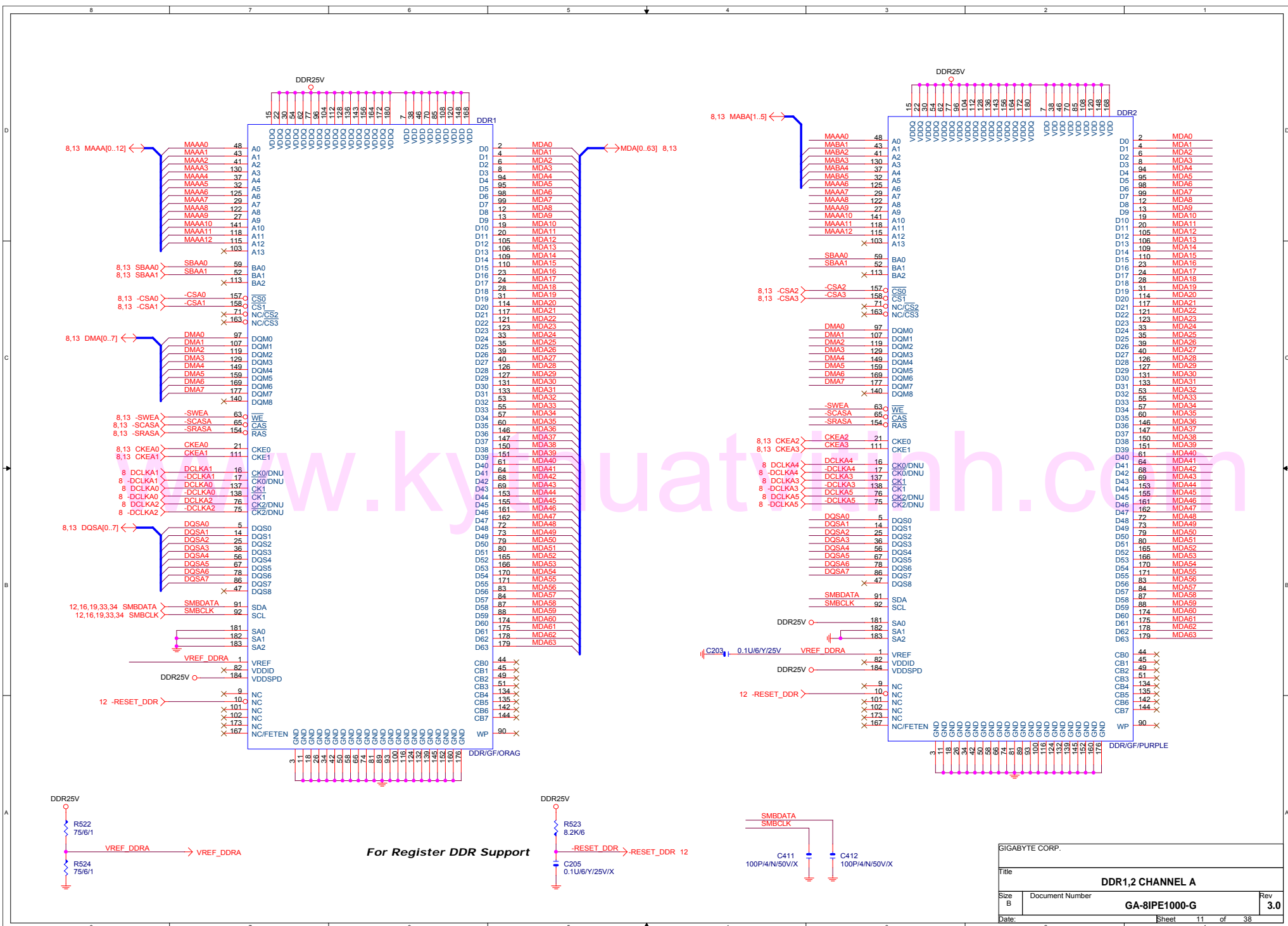
Place mid of bus trace

10 mil trace with 7 mil space

Title		
SPRINGDALE AGP,HUB,CSA,VGA		
Size	Document Number	Rev
Custom	GA-8IPE1000-G	3.0
Date:	Sheet 9 of 38	

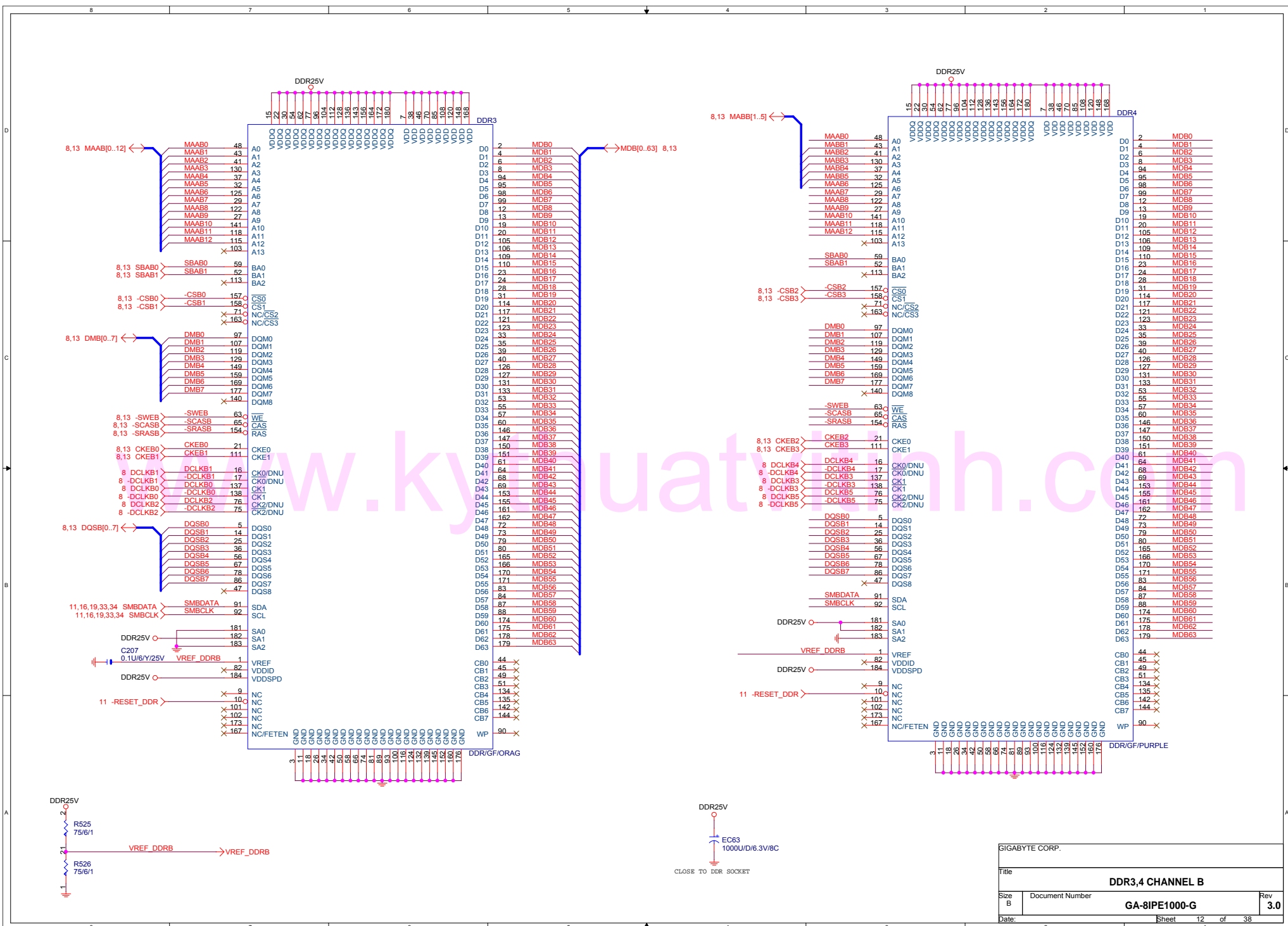


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SPRINGDALE PWR			
Size	Document Number	Rev	
Custom	GA-8IPE1000-G	3.0	
Date:	Sheet 10 of 38		



For Register DDR Support

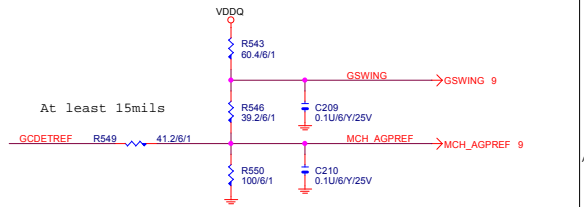
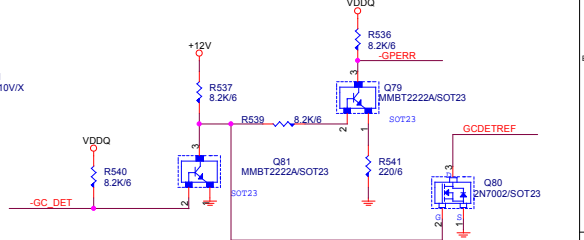
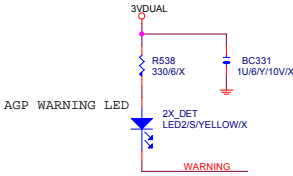
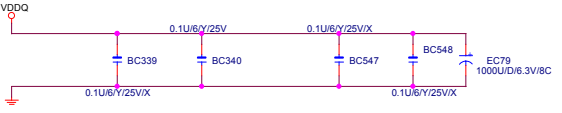
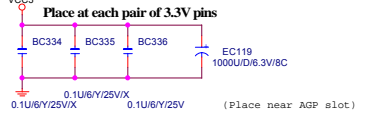
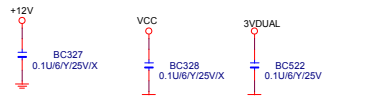
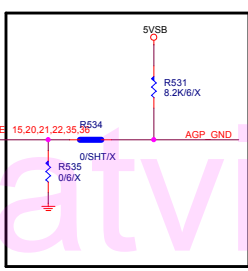
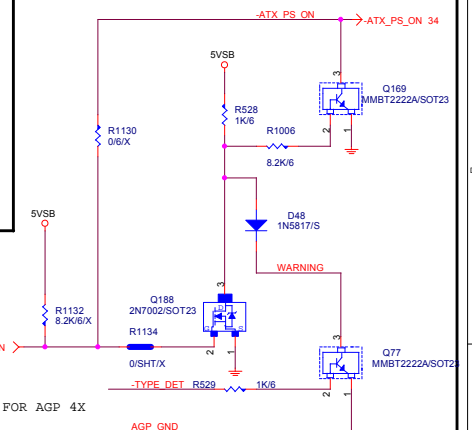
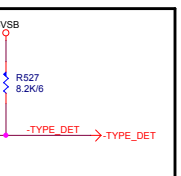
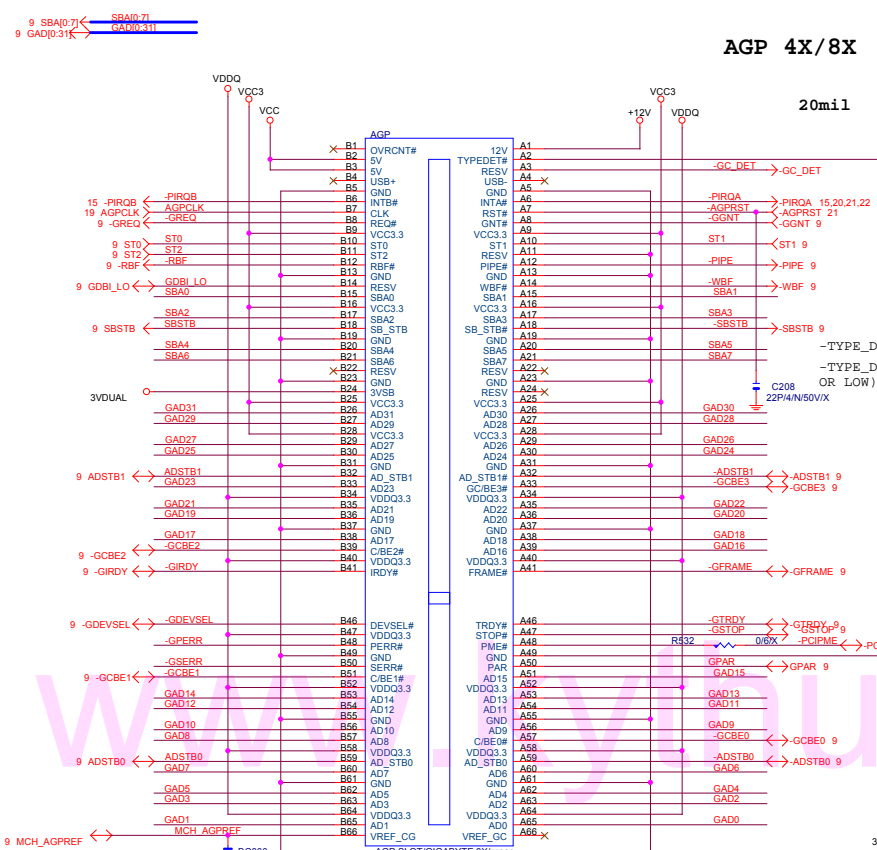
SIGABYTE CORP.		
Title		
DDR1,2 CHANNEL A		
Size	Document Number	Rev
B	GA-8IPE1000-G	3.0
Date:	Sheet 11 of 38	



SIGABYTE CORP.		
Title		
DDR3,4 CHANNEL B		
Size	Document Number	Rev
B	GA-8IPE1000-G	3.0
Date:	Sheet 12 of 38	

AGP 4X/8X

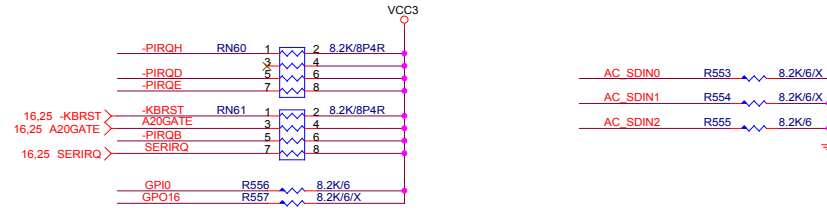
20mil



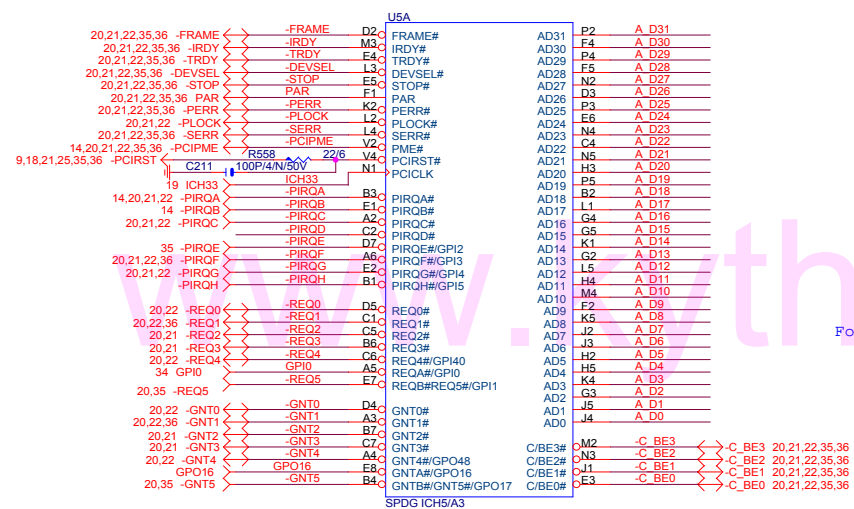
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33

GIGABYTE CORP.

Title			Rev
AGP SLOT			
Size	Document Number	Rev	
Customer	GA-8IPE1000-G	3.0	
Date	日期: 二月 05, 2004	Sheet	14 of 38

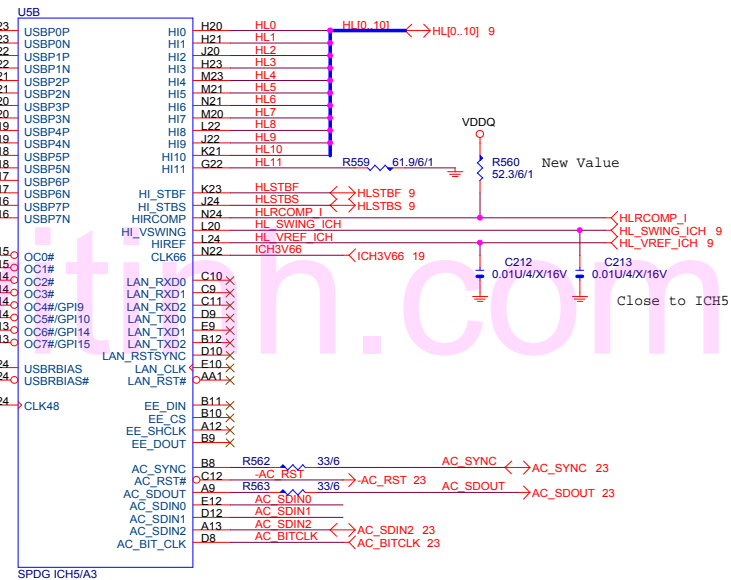


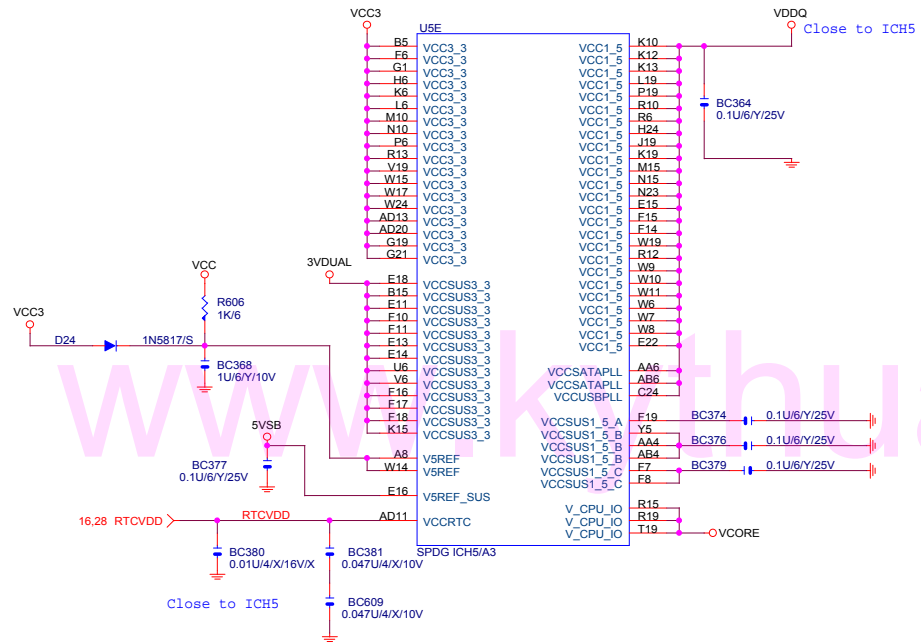
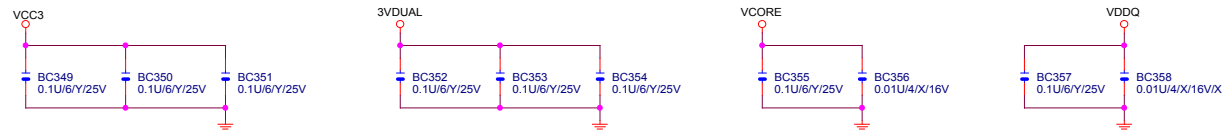
A_D0_311 <-> A_D0[.31] 20,21,22,35,36

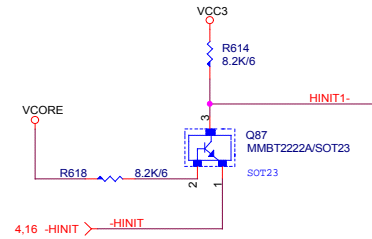
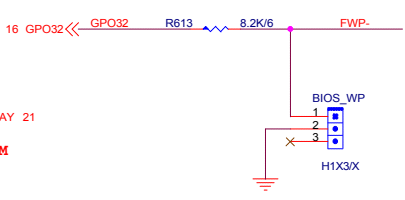
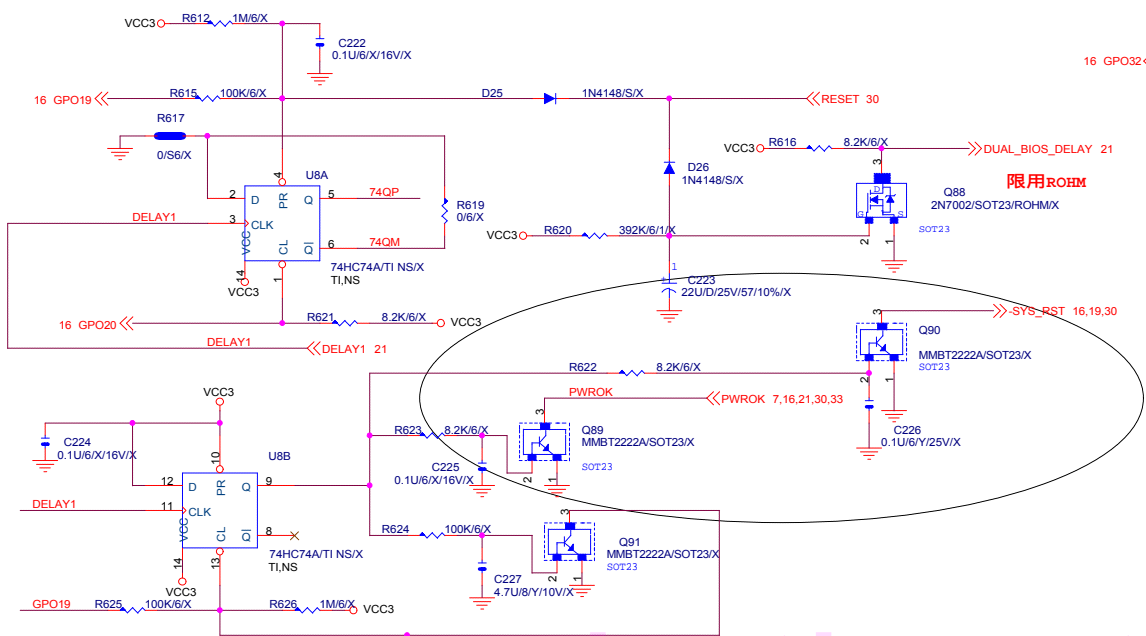


Follow Intel Layout

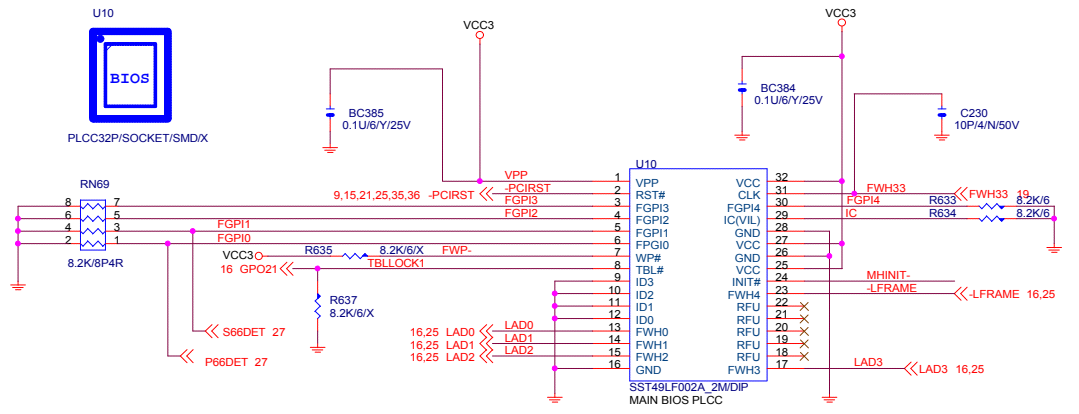
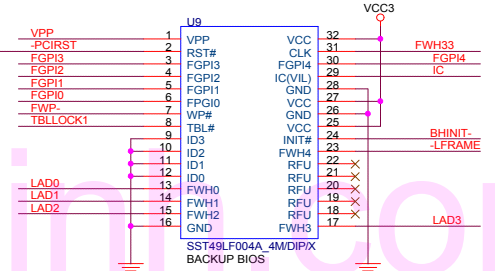
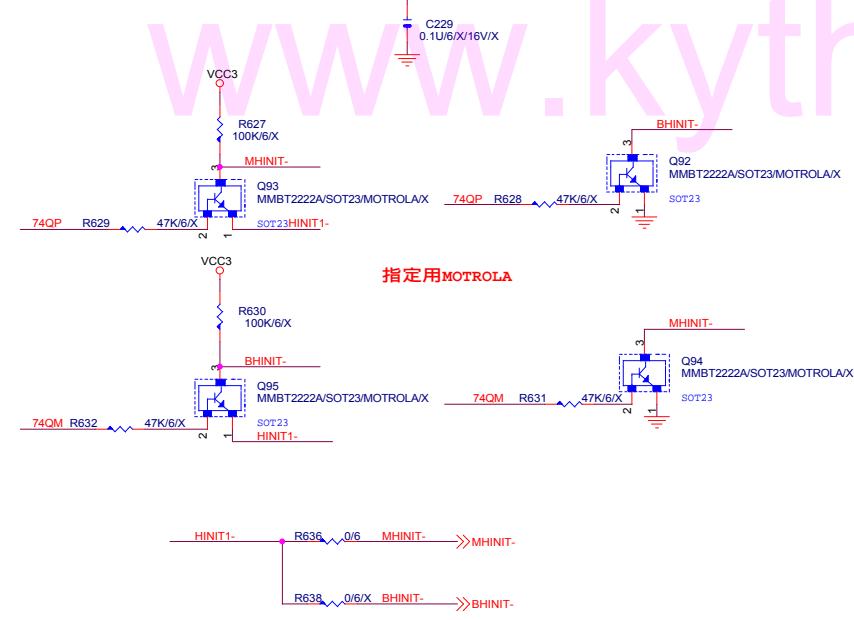
Less than 500mils from ICH5







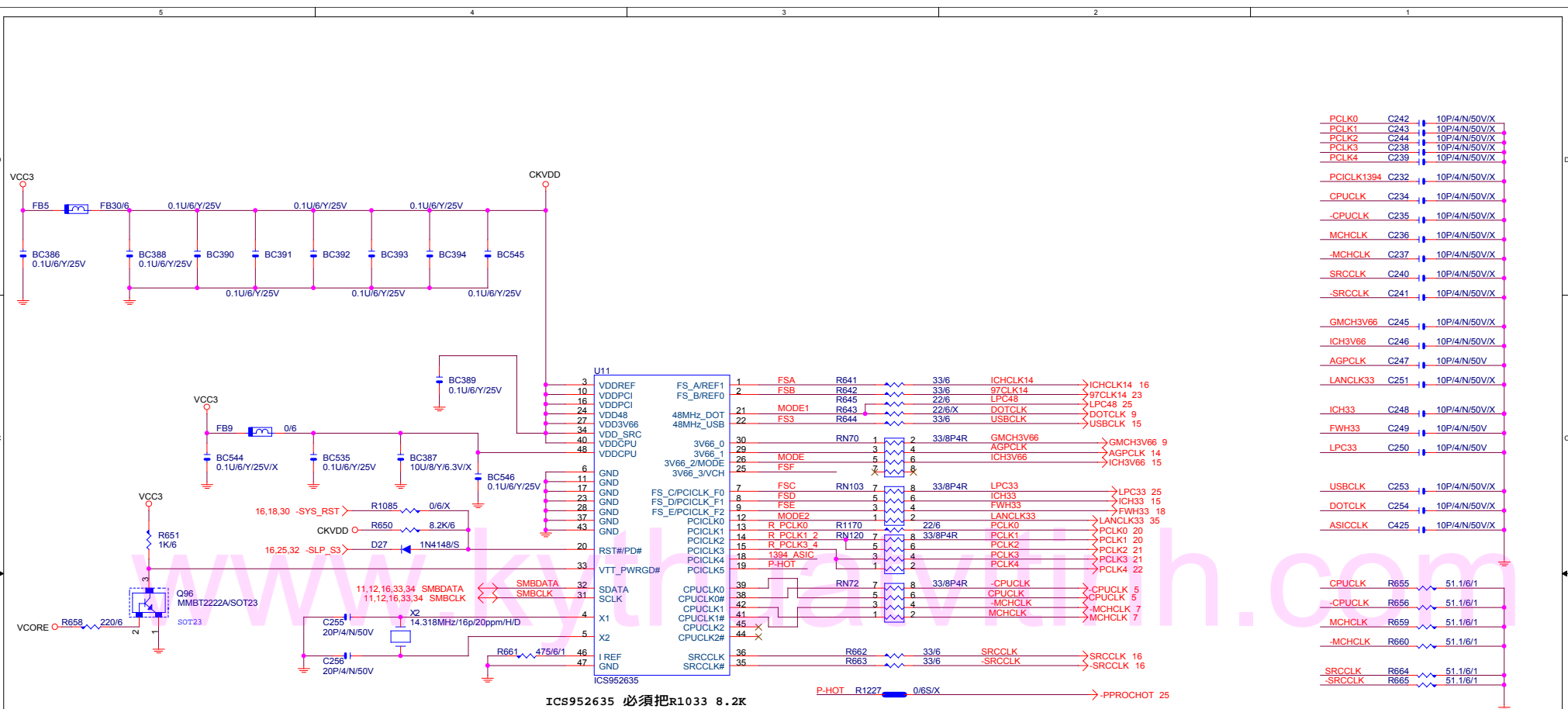
BIOS_WP:	
1-2	WRITE PROTECT
2-3	DISABLE



GIGABYTE CORP.		
Title		
FWH		
Size	Document Number	Rev
B	GA-8IPE1000-G	3.0
Date:	星期四, 二月 05, 2004	Sheet 18 of 38

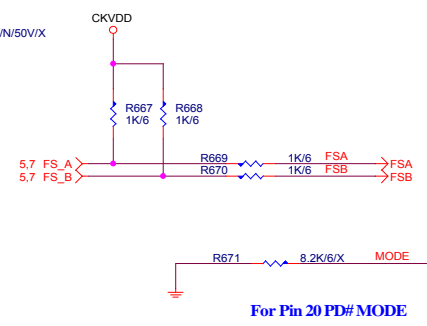
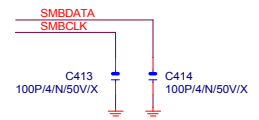
ADD WINBOUD FWH SEC. SOURCE

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- PCLK0 C242 10P/4/N/50V/X
- PCLK1 C243 10P/4/N/50V/X
- PCLK2 C244 10P/4/N/50V/X
- PCLK3 C238 10P/4/N/50V/X
- PCLK4 C239 10P/4/N/50V/X
- PCICLK1394 C232 10P/4/N/50V/X
- CPUCCLK C234 10P/4/N/50V/X
- CPUCCLK C235 10P/4/N/50V/X
- MCHCLK C236 10P/4/N/50V/X
- MCHCLK C237 10P/4/N/50V/X
- SRCCCLK C240 10P/4/N/50V/X
- SRCCCLK C241 10P/4/N/50V/X
- GMCH3V66 C245 10P/4/N/50V/X
- ICH3V66 C246 10P/4/N/50V/X
- AGPCLK C247 10P/4/N/50V
- LANCLK33 C251 10P/4/N/50V/X
- ICH33 C248 10P/4/N/50V/X
- FWH33 C249 10P/4/N/50V
- LPC33 C250 10P/4/N/50V
- USBCLK C253 10P/4/N/50V/X
- DOTCLK C254 10P/4/N/50V/X
- ASICCLK C425 10P/4/N/50V/X
- CPUCCLK R655 51.1/6/1
- CPUCCLK R656 51.1/6/1
- MCHCLK R659 51.1/6/1
- MCHCLK R660 51.1/6/1
- SRCCCLK R664 51.1/6/1
- SRCCCLK R665 51.1/6/1

ICS952635 必須把R1033 8.2K REMOVE



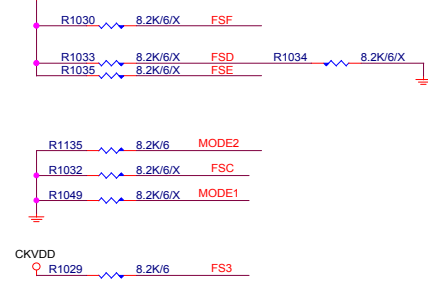
CYPRESS CY28405

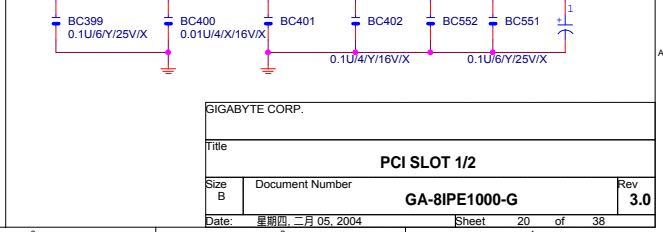
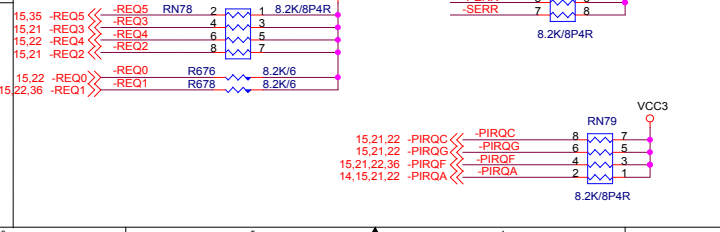
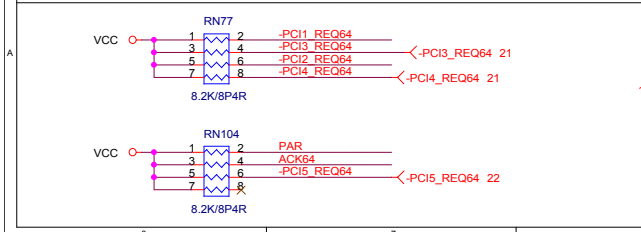
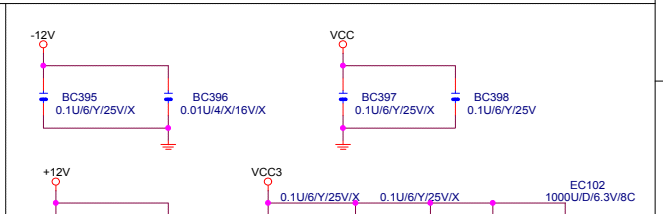
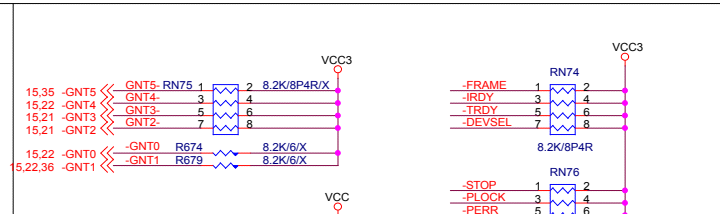
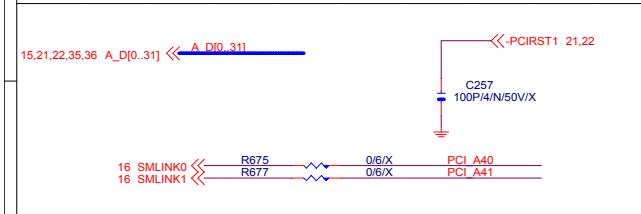
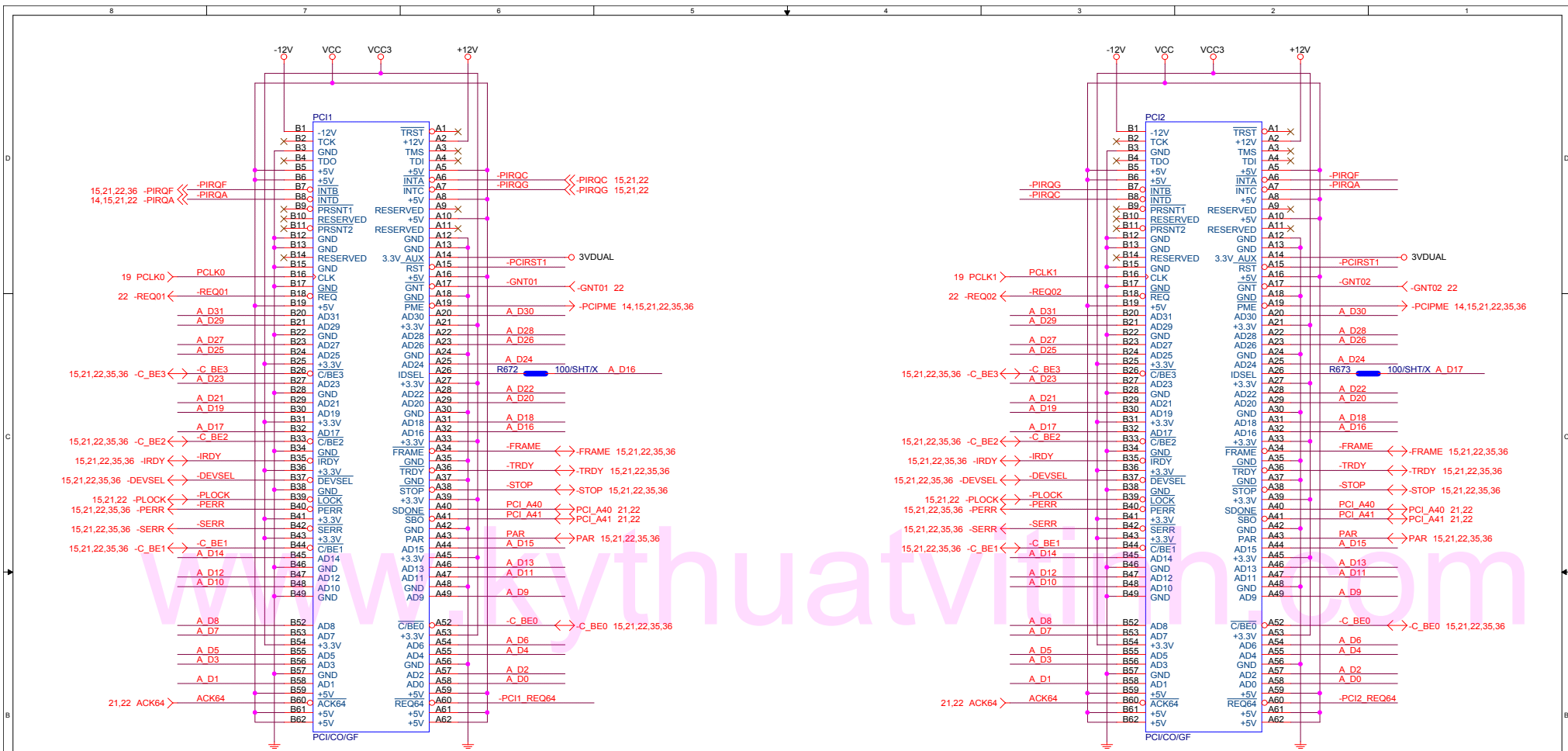
FS_E	FS_D	FS_C	FS_B	FS_A	Clock
1	1	0	0	0	100.9MHz
1	1	0	0	1	133.9MHz
1	1	0	1	1	166.9MHz
1	1	0	1	0	200.9MHz

ICS952616

FS_E	FS_3	FS_C	FS_B	FS_A	Clock
1	0	0	0	0	100MHz
1	0	0	0	1	133MHz
1	0	0	1	1	166MHz
1	0	0	1	0	200MHz

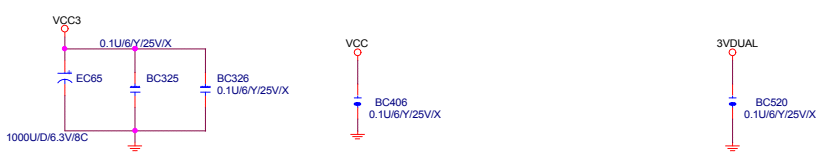
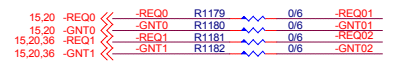
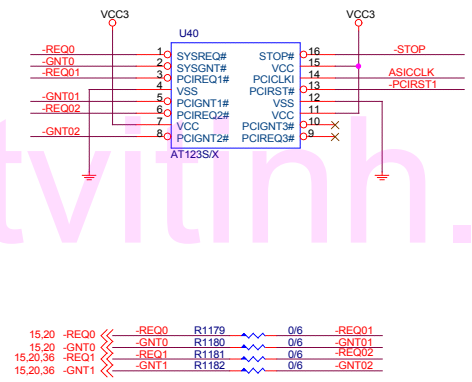
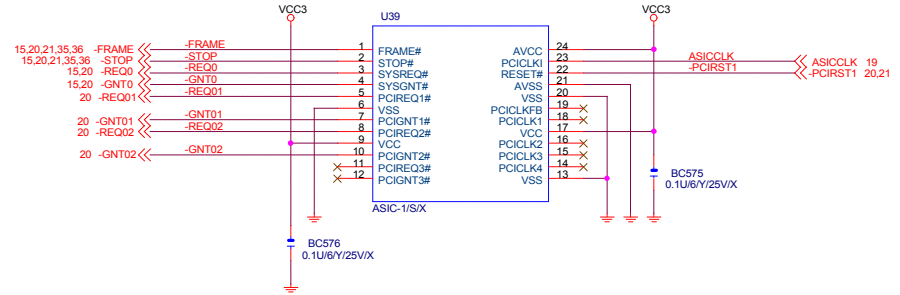
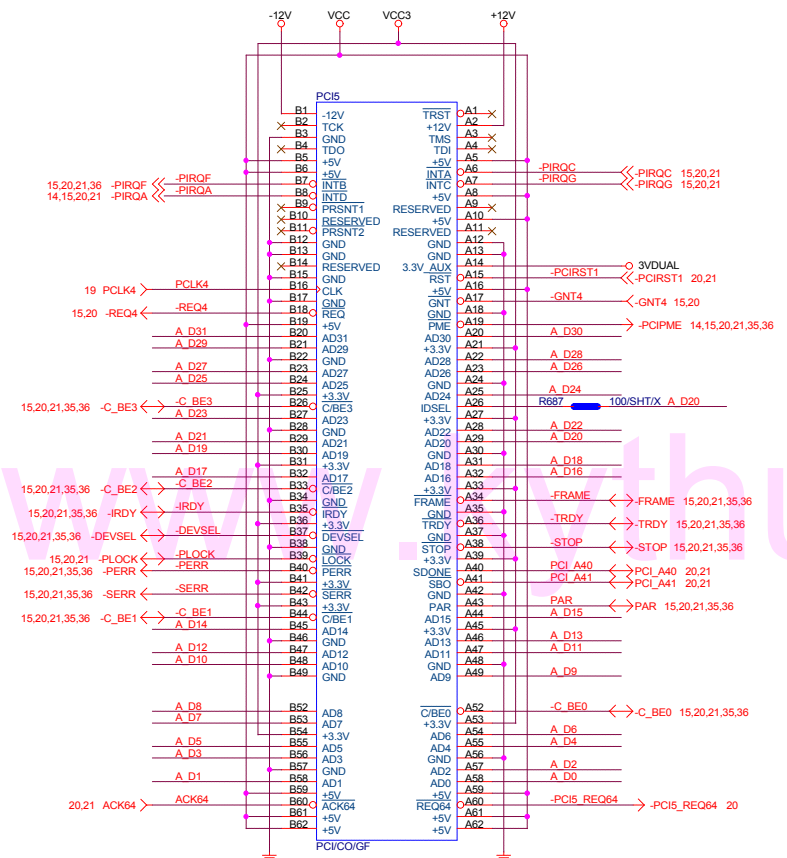
ICS + CYPRESS CO-LAYOUT





GIGABYTE CORP.		
Title		
PCI SLOT 1/2		
Size	Document Number	Rev
B	GA-8IPE1000-G	3.0
Date:	日期: 二月 05, 2004	Sheet 20 of 38

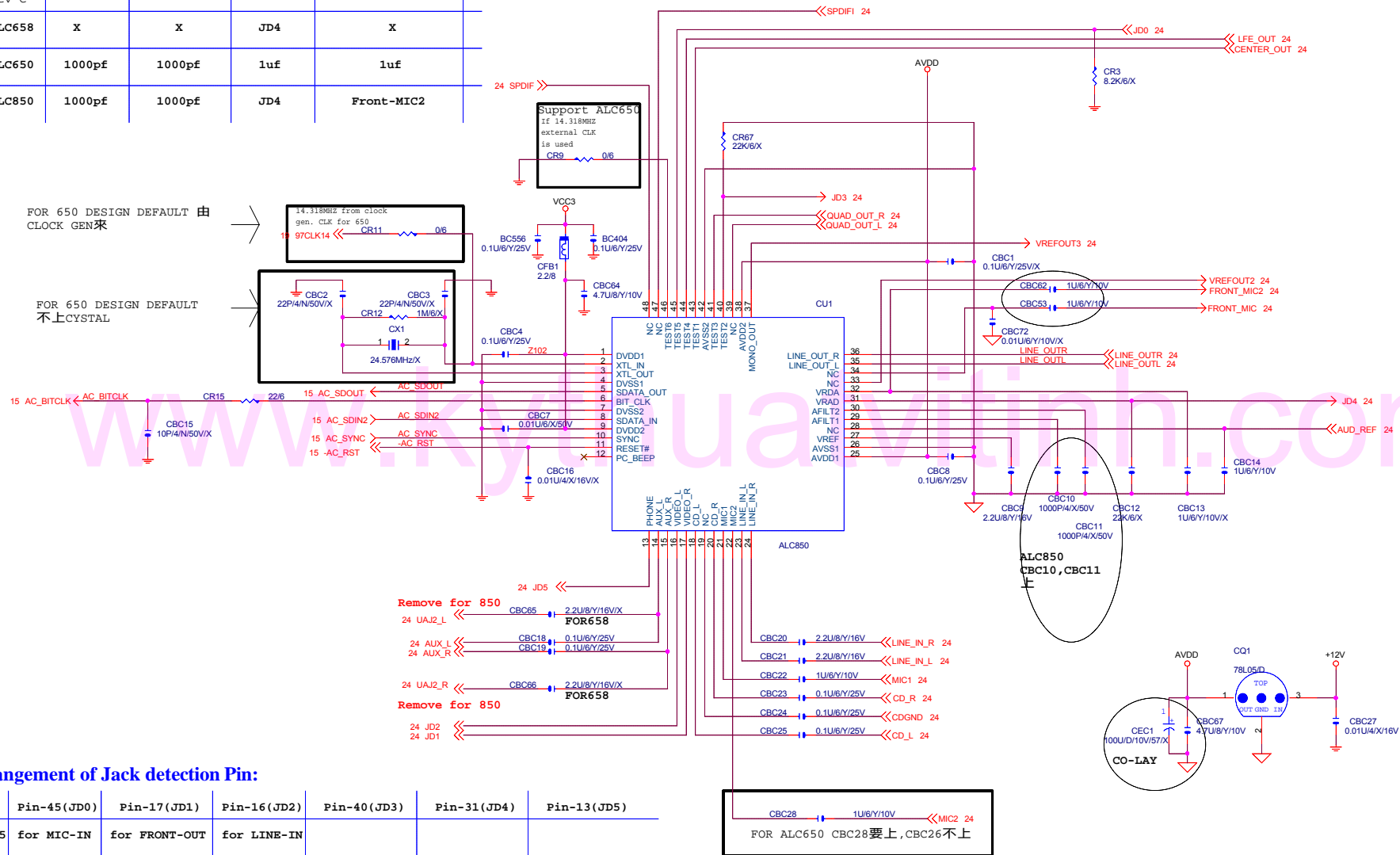
15,20,21,35,36_A_D[0..31] << A_D[0..31]



GIGABYTE CORP.			
Title			
PCI SLOT 5			
Size	Document Number	Rev	
Custom	GA-8IPE1000-G	3.0	
Date:	日期: 二月 05, 2004	Sheet	22 of 38

Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2

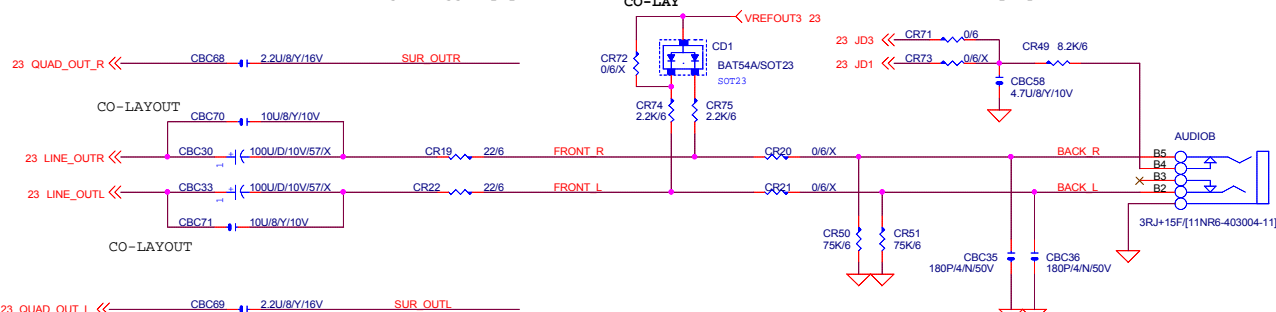


Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

LINE OUT

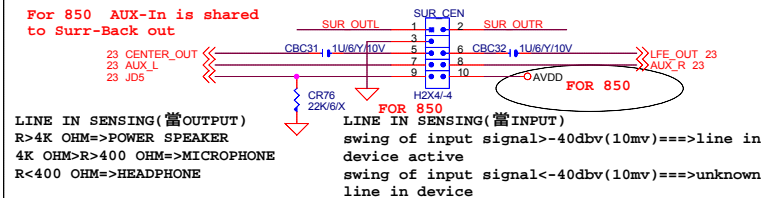
JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual) 1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



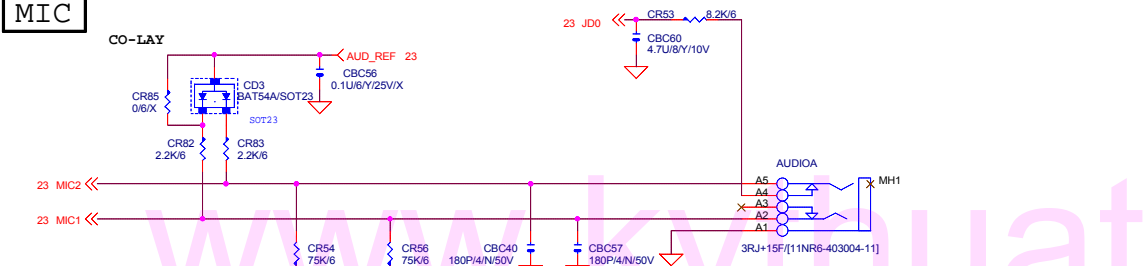
LINE OUT SENSING
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

2x5 header for 850
 For 850 if JD5 = low AUX-In is configured as input
 For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

For 850 AUX-In is shared to Surr-Back out



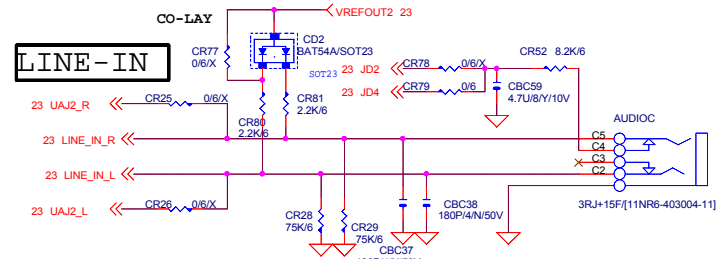
MIC



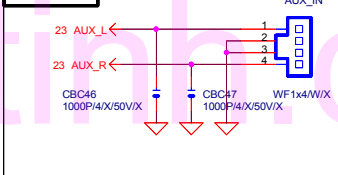
MICROPHONE IN SENSING(當INPUT) (利用vref 偏壓 與CR43,CR32 並聯求出阻抗)
 7.1k ohm>R>2.3k ohm==>microphone in
 R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

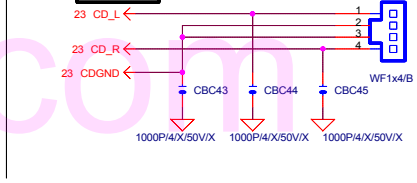
LINE-IN



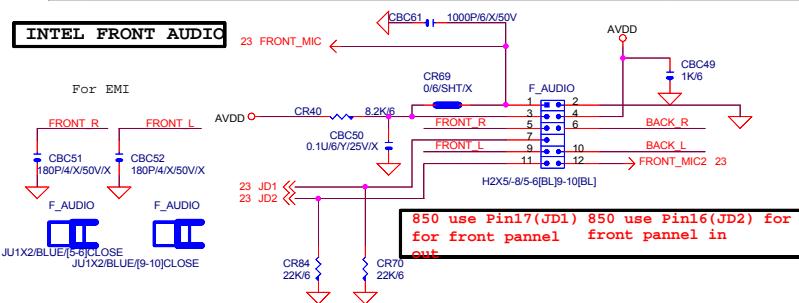
AUX IN DEFAULT NO POP



CD IN

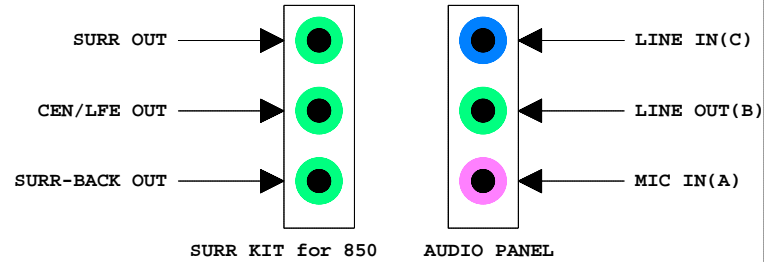
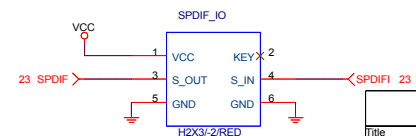


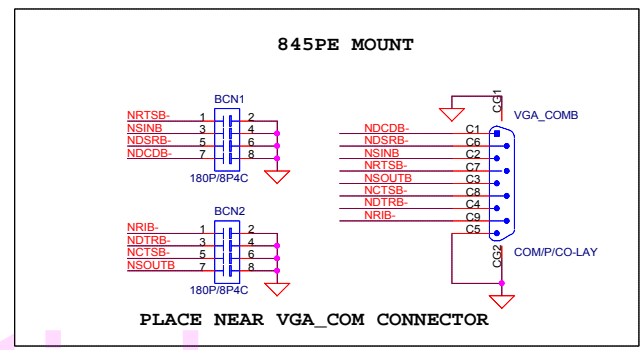
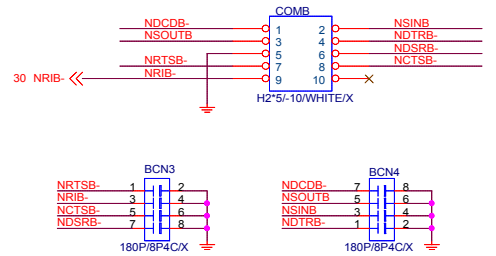
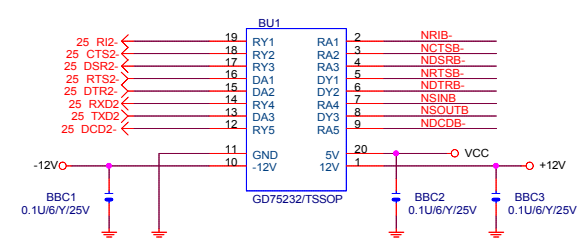
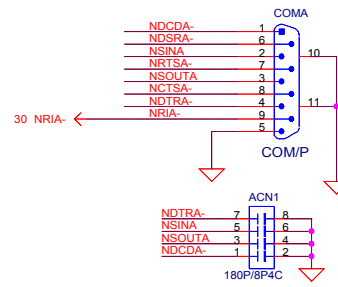
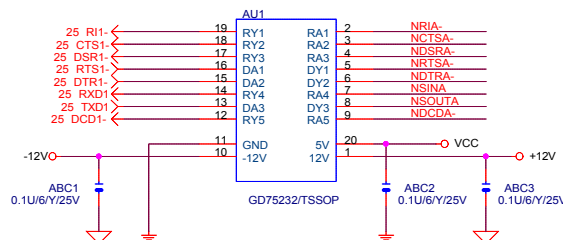
INTEL FRONT AUDIO



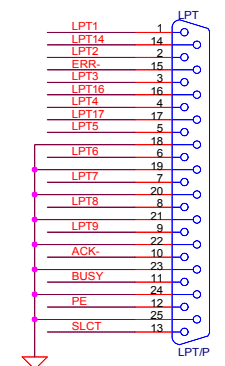
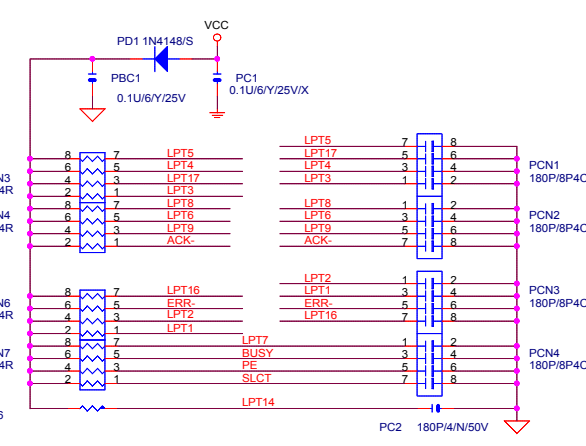
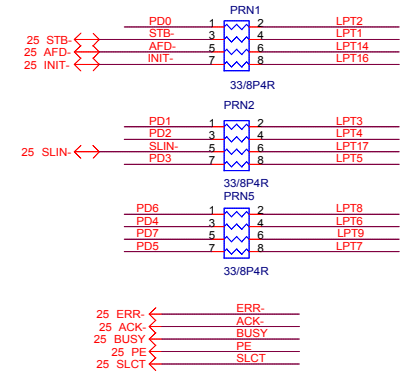
850 use Pin17(JD1) 850 use Pin16(JD2) For front panel front panel in out

SPDIF_IO

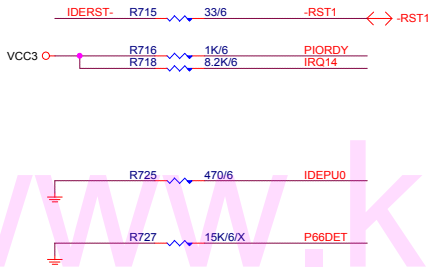
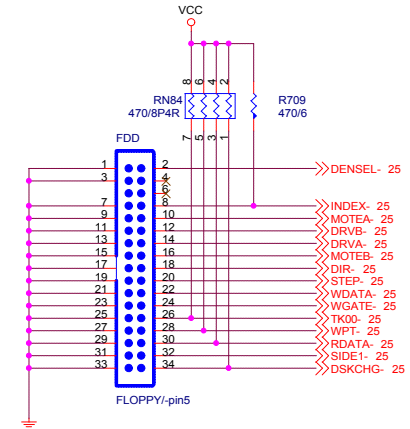
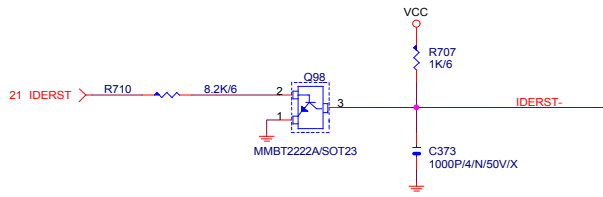




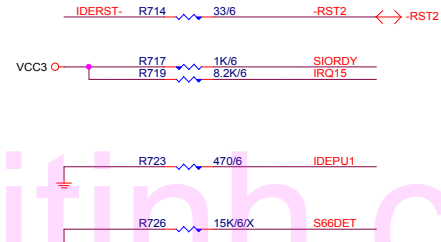
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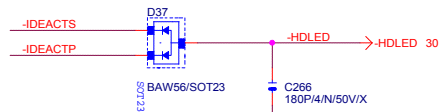
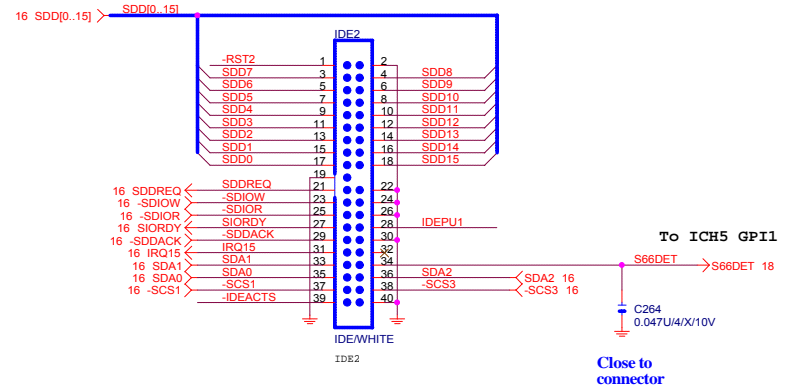
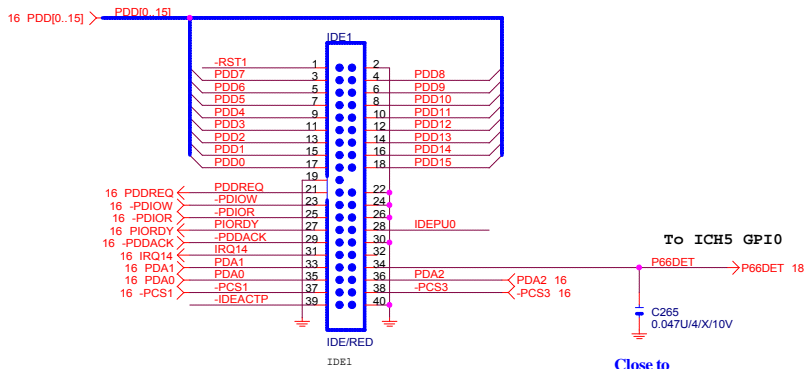
SIGABYTE CORP.		
Title		
COM & IR & LPT PORT & FLOOPY		
Size B	Document Number	Rev
	GA-8IPE1000-G	3.0
Date:	星期四, 三月 05, 2004	Sheet 26 of 38



PRIMARY IDE CONNECTOR

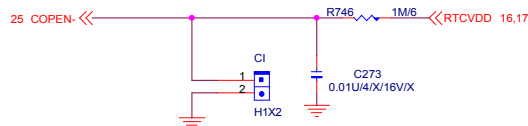
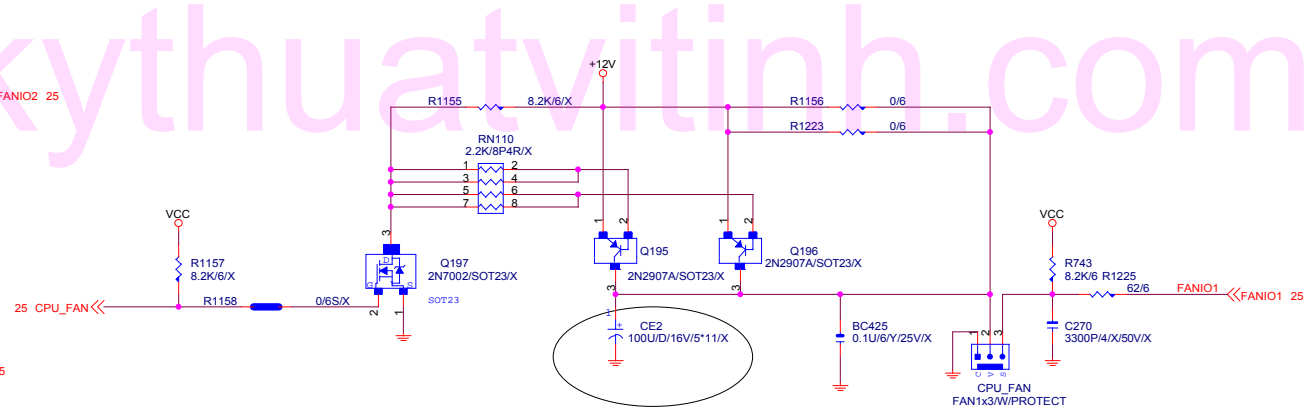
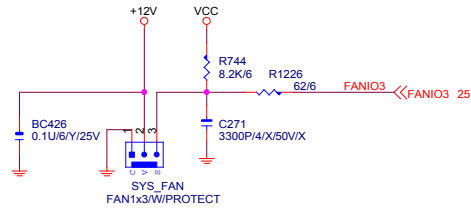
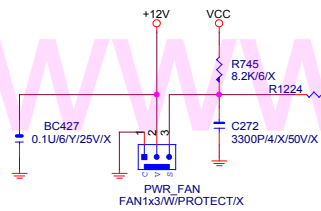
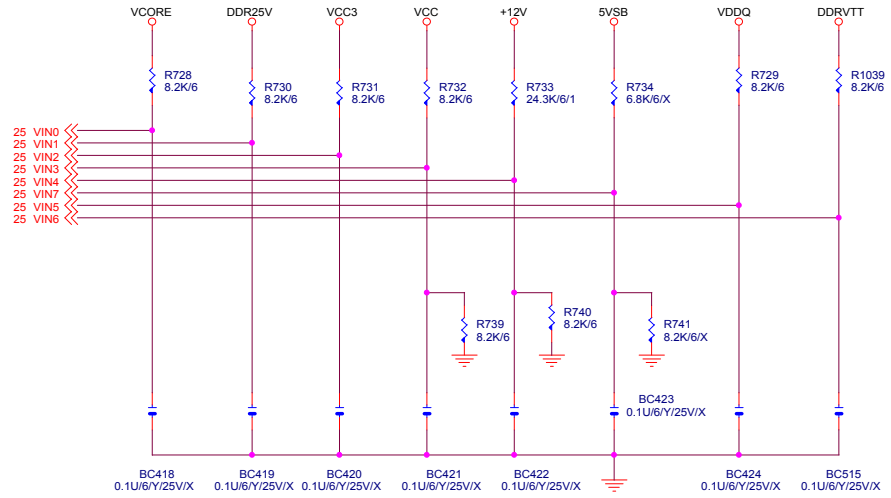
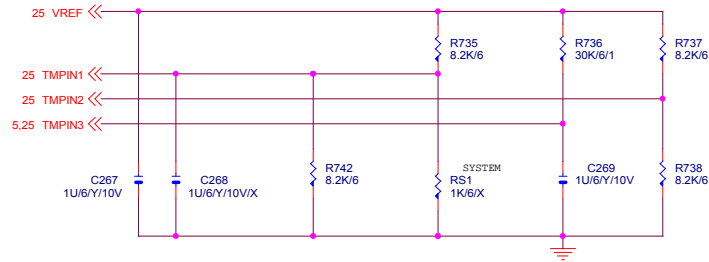


SECONDARY IDE CONNECTOR

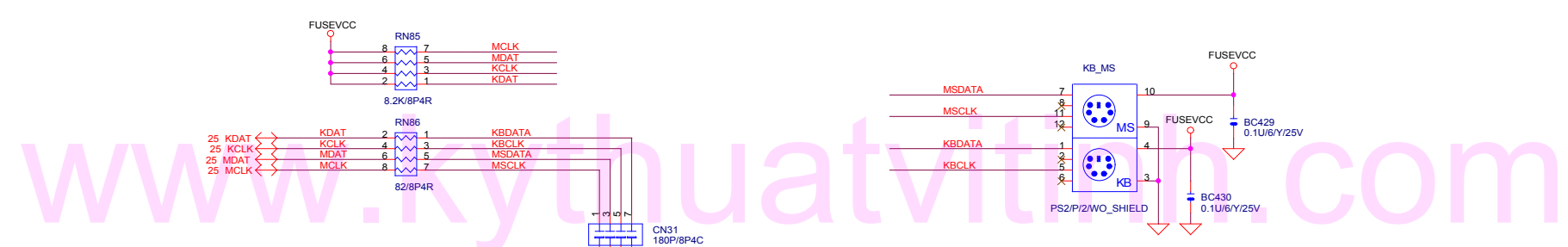
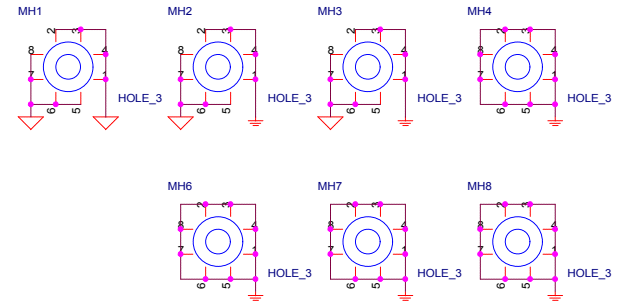
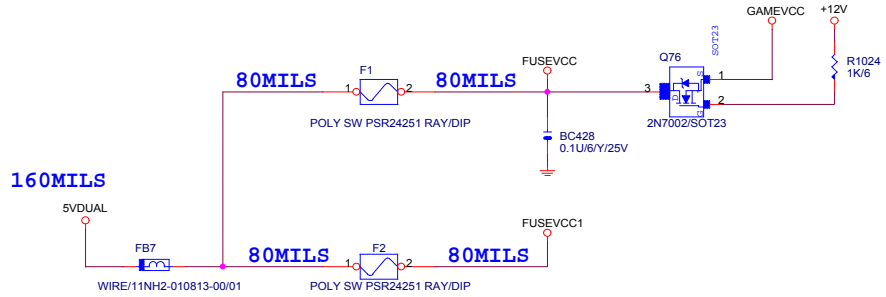


GIGABYTE CORP.		
Title		
IDE CONNECTOR		
Size	Document Number	Rev
B	GA-8IPE1000-G	3.0
Date:	Sheet	of
	27	38

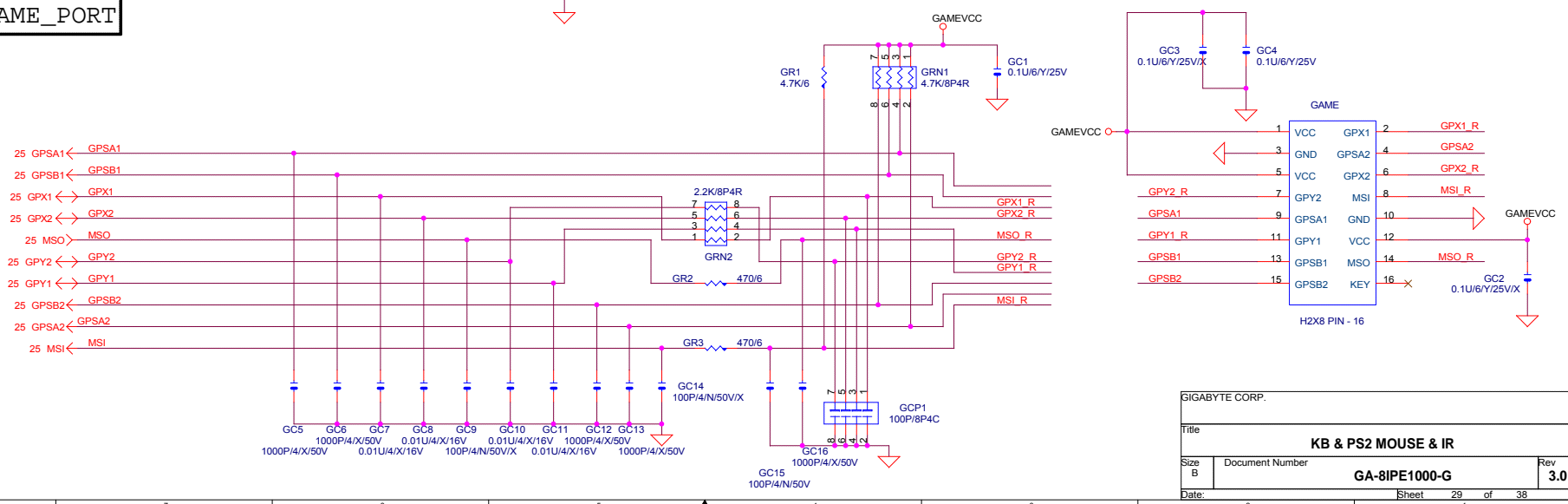
Hardware Monitor circuits



SIGABYTE CORP.		
Title		
FAN/HWMO		
Size B	Document Number	Rev
	GA-8IPE1000-G	3.0
Date:	星期四, 二月 05, 2004	Sheet 28 of 38

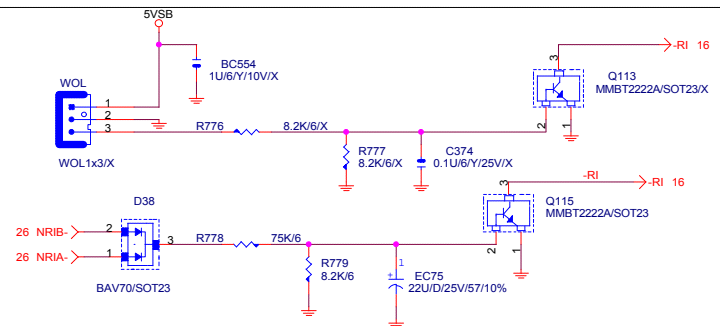
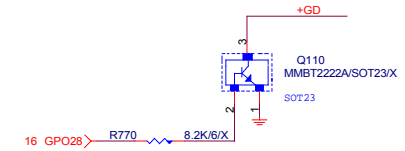
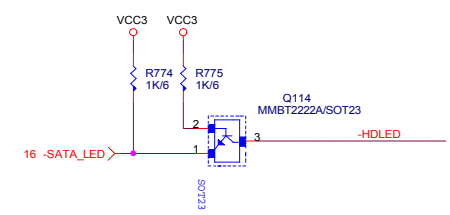
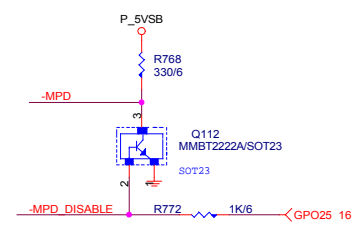
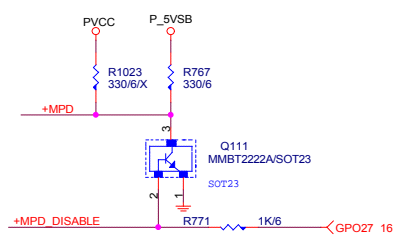
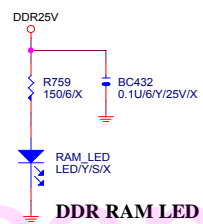
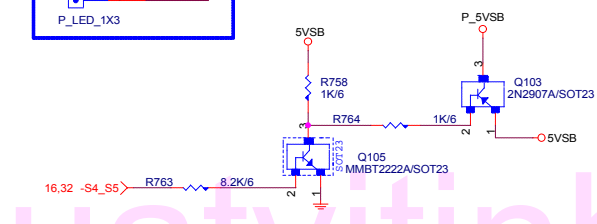
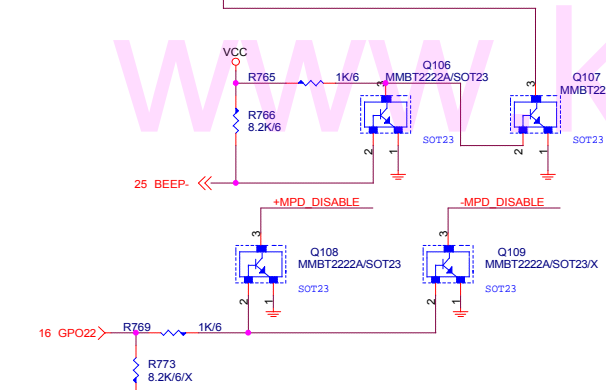
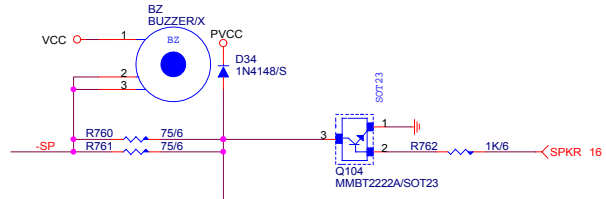
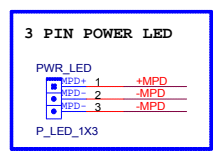
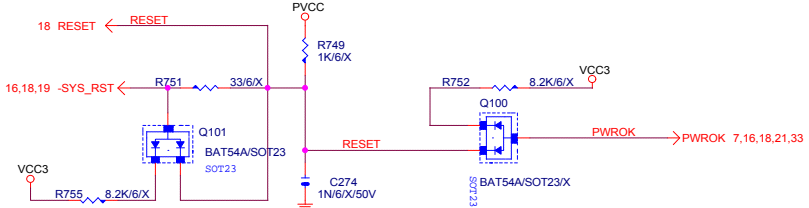
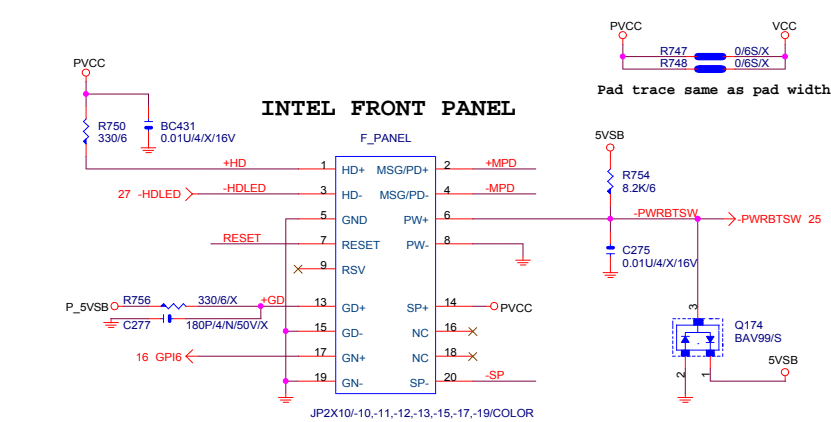


GAME_PORT



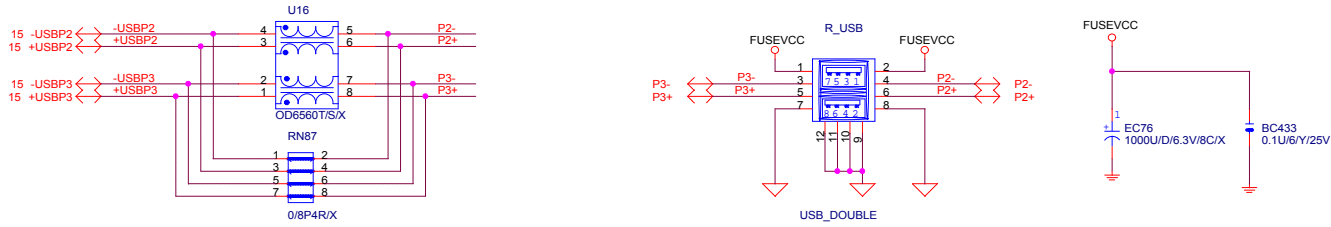
SIGABYTE CORP.		
Title		
KB & PS2 MOUSE & IR		
Size	Document Number	Rev
B	GA-8IPE1000-G	3.0
Date:	Sheet	of
	29	38

INTEL FRONT PANEL

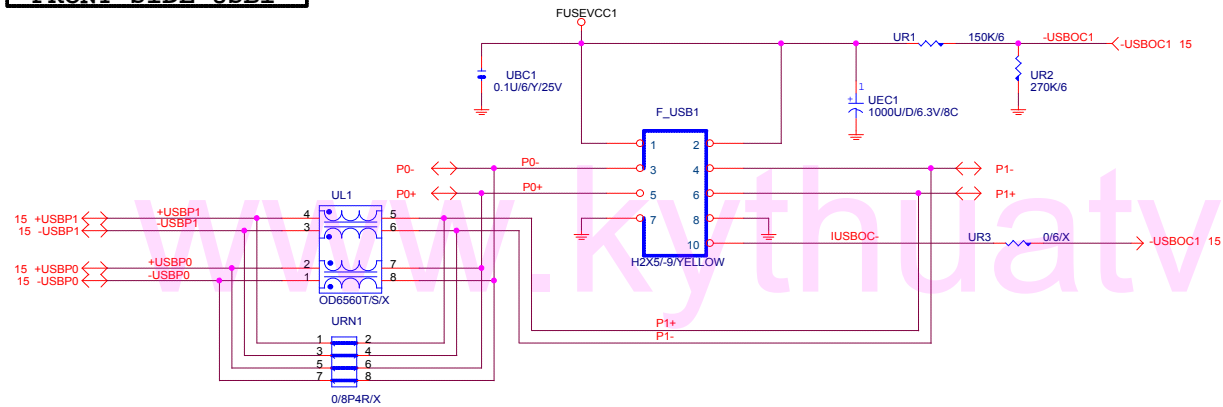


GIGABYTE CORP.		
Title		
PANEL & STR LED & RI		
Size B	Document Number	Rev
	GA-8IPE1000-G	3.0
Date:	Sheet	30 of 38

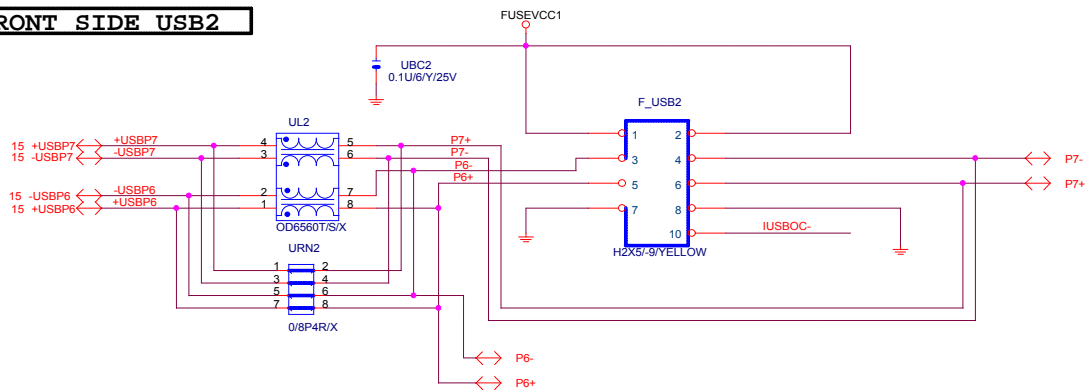
REAR USB



FRONT SIDE USB1

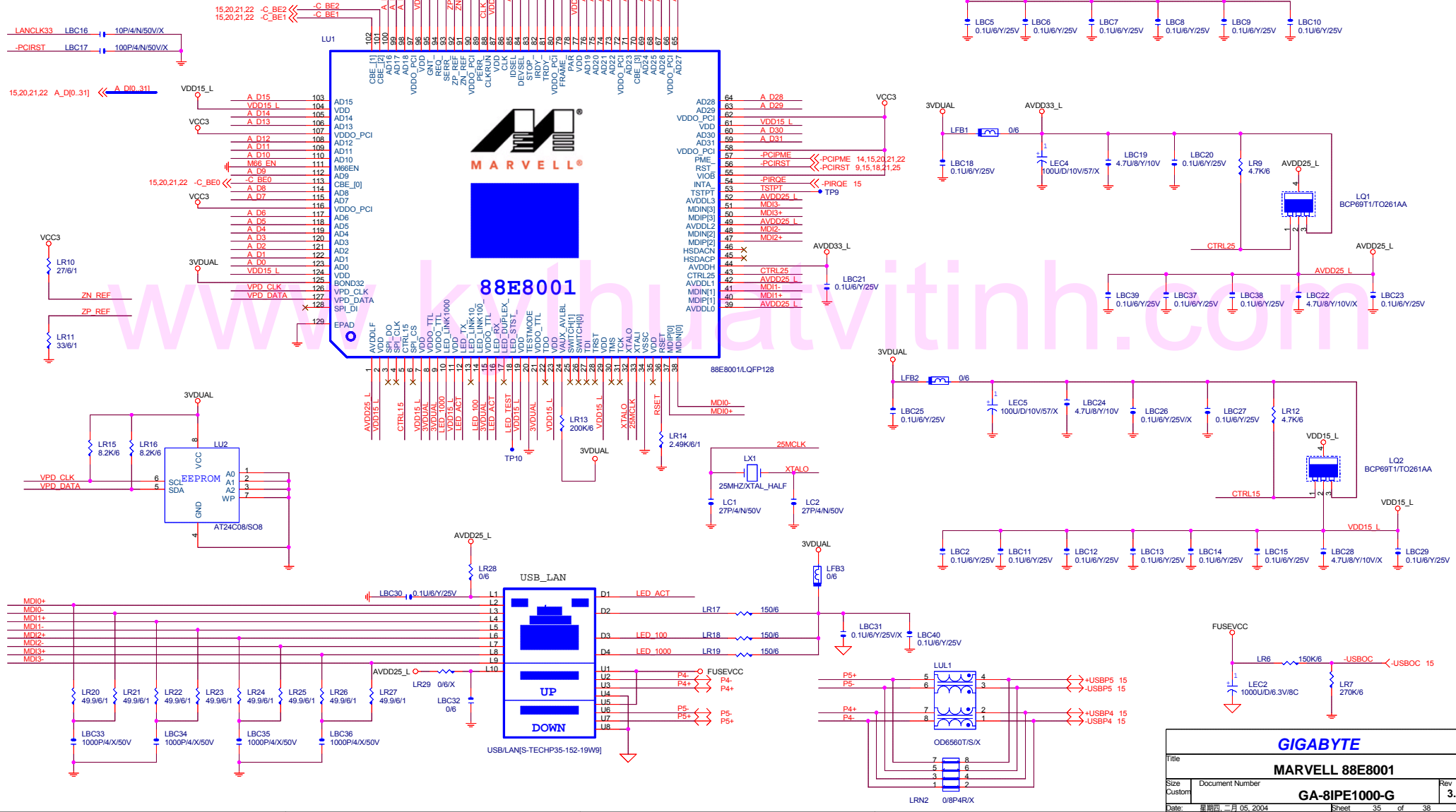


FRONT SIDE USB2



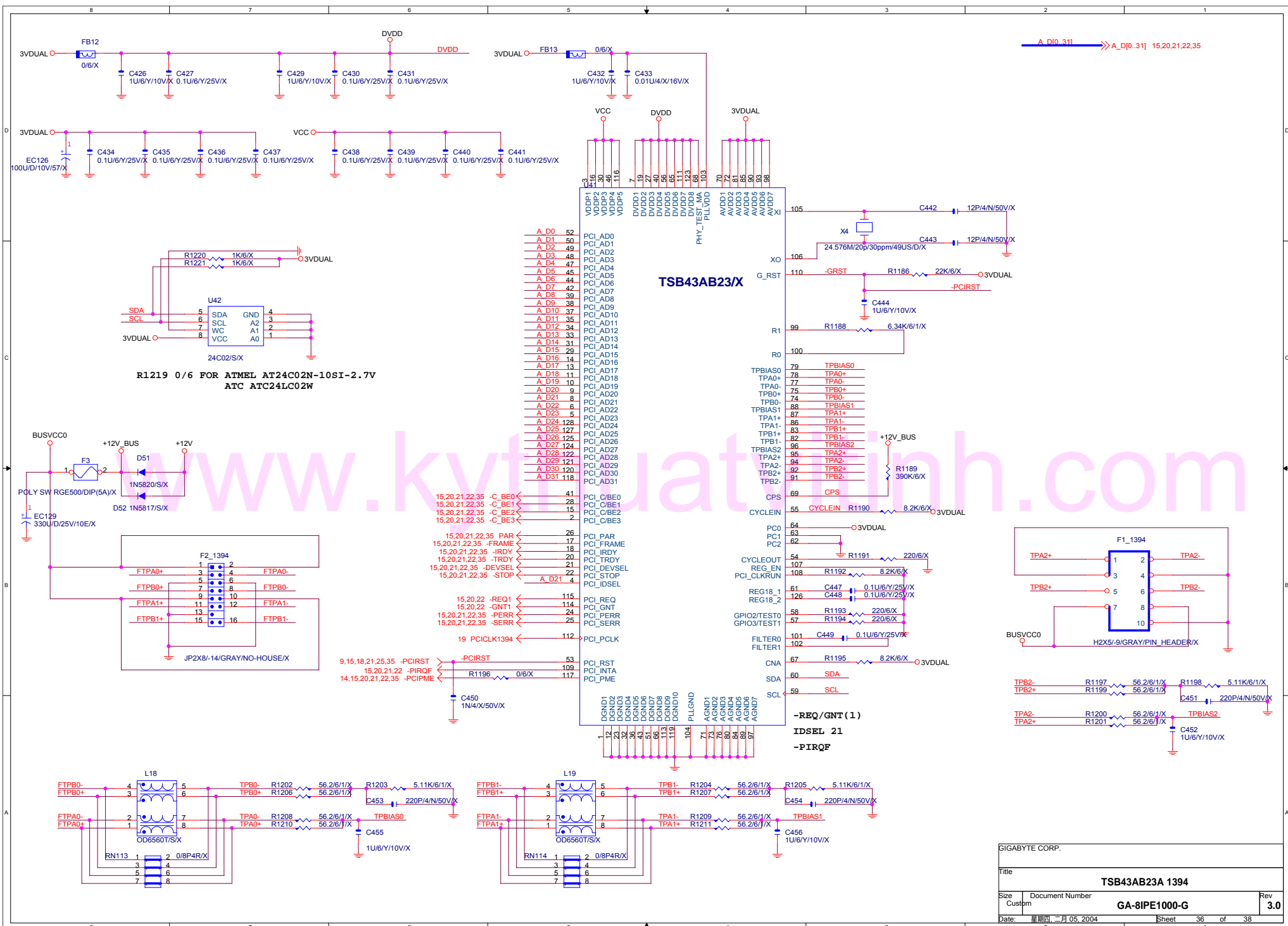
GIGABYTE CORP.		
Title		
ICH USB PORT		
Size B	Document Number	Rev
	GA-8IPE1000-G	3.0
Date:	Sheet	of
	31	38

- # Layout Check 注意事項
1. LU1 PIN129 需下內層GND, 至少打 22 VIA
 2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
 3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
 4. MDI正負0-3, TRACE 8:7:8, 每對之間保持 40mil



POWER DECOUPLING CAP.

Title		
MARVELL 88E8001		
Size	Document Number	Rev
Custom	GA-8IPE1000-G	3.0
Date:	日期: 二月 05, 2004	Sheet 35 of 38



SIBABYTE CORP.		
Title		
TSB43AB23A 1394		
Size	Document Number	Rev
Custom	GA-8PE1000-G	3.0
Date:	星期四, 二月 05, 2004	Sheet 36 of 38

GIGABYTE GA-8IPE1000-G PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK0	-REQ01	-GNT01
PCI SLOT2	17	F,G,A,C	PCLK1	-REQ02	-GNT02
PCI SLOT3	18	G,A,C,F	PCLK2	-REQ2	-GNT2
PCI SLOT4	19	A,C,F,G	PCLK3	-REQ3	-GNT3
PCI SLOT5	20	C,F,G,A	PCLK4	-REQ4	-GNT4
TI 1394	21	F	PCICLK1394	-REQ1	-GNT1
LAN (Marvell)	25	E	LANCLK33	-REQ5 (REQB#)	-GNT5 (GNTB#)

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Title PCI ROUNT LIST			
Size	Document Number	GA-8IPE1000-G	Rev 3.0
Custom	Date: 星期四, 二月 05, 2004		Sheet 37 of 38

